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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte KAZUTOSHI TSUYUTANI[1]

Appeal 2018-003114
Application 14/054,556
Technology Center 2800

Before BRADLEY W. BAUMEISTER, SHARON FENICK, and DAVID J. CUTITTA II, *Administrative Patent Judges*.

BAUMEISTER, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1–3, 5–8, 13, 15, and 21–31, which constitute all the claims pending in this application. App. Br. 1. We have jurisdiction under 35 U.S.C. § 6(b). Oral argument was held on September 9, 2019. A transcript will be entered into the record in due course.

We AFFIRM.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant lists TDK Corporation as the real party in interest. Appeal Brief filed August 11, 2017 ("App. Br.") 1.

STATEMENT OF THE CASE

Appellant describes the present invention as follows:

> Disclosed herein is a circuit board that includes a resin substrate including a substrate wiring layer, and an electronic component embedded in the resin substrate and having a plurality of external electrodes. The resin substrate includes a plurality of via holes that expose the external electrodes and a plurality of via conductors embedded in the via holes to electrically connect the substrate wiring layer to the external electrodes. At least some of the via holes are different in planar shape from each other.

Abstract.

Independent claim 1 illustrates the subject matter of the appealed claims:

> 1. A circuit board, comprising:
>
> a resin substrate including a substrate wiring layer, the substrate wiring layer being an uppermost wiring layer of the circuit board; and
>
> an electronic component embedded in the resin substrate and including a plurality of chip wiring layers stacked one another, the chip wiring layers including a first wiring layer that is an uppermost one of the chip wiring layers and a second wiring layer that is located below the first wiring layer, the first wiring layer including a plurality of external electrodes, the external electrodes including a first external electrode,
>
> wherein the resin substrate includes a plurality of via holes that directly connect surfaces of the external electrodes to the substrate wiring layer and a plurality of via conductors embedded in the via holes to electrically connect the substrate wiring layer to the external electrodes, at least some of the via holes being different in planar shape from each other,
>
> wherein the first external electrode includes a first section contacting one of the via conductors and a second section contacting an internal via conductor that com1ects the first external electrode to the second wiring layer, and

> wherein the second section is in contact with a resin layer included in the resin substrate without an intervention of [another] layer.

THE REJECTIONS

Claims 1–7, 21–24, and 28–31 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Kikuchi et al. (US 2013/0026632 A1; published Jan. 31, 2013) ("Kikuchi"), Hurwitz (US 2013/0319747 A1; published Dec. 5, 2013), and Tanaka (US 2009/0242252 A1; published Oct. 1, 2009). Final Act. 3–10.[2]

Claims 13, 14, and 25–27 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Kikuchi, Feng et al. (US 5,081,563; issued Jan. 14, 1992) ("Feng"), and Tanaka. Final Act. 10–13.

Claim 15 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Kikuchi, Feng, and Hurwitz. Final Act. 14–15.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Kikuchi, Hurwitz, and Kikuchi (JP 2012-009602; published Jan. 12, 2012) ("Kikuchi '602"). Final Act. 15–16.

The Examiner finds that Kikuchi discloses most of the limitations of claim 1 with a couple of exceptions. Final Act. 3–4. For example, the Examiner finds that Kikuchi suggests that some of the resin substrate's via holes have different shapes, but does not disclose via holes being different in *planar* shape from each other. *Id.* at 4 (citing resin substrate vias 104, 142,

[2] Rather than repeat the Examiner's positions and Appellant's arguments in their entirety, we refer to the above-mentioned Appeal Brief, as well as the following documents, for their respective details: the Final Action mailed March 16, 2017 ("Final Act."); the Examiner's Answer mailed December 13, 2017 ("Ans."); and the Reply Brief filed January 31, 2018 ("Reply Br.").

and 301, which are depicted, e.g., in Kikuchi FIG. 9). The Examiner relies on Hurwitz for teaching this limitation. *Id.* (citing Hurwitz FIG. 3, vias 304, 306, 308, 316, and 320). The Examiner further determines that motivation existed to modify the shape of Kikuchi's vias. *Id.* at 4–5.

The Examiner further finds that although "Kikuchi suggests the whole wiring layer 21 being exposed on [the] top surface of the semiconductor chip (*id.* at 5 (citing Kikuchi FIG. 10B)), "Kikuchi does not explicitly disclose . . . wherein the second section [of the electronic component's external electrode] is in contact with a resin layer included in the resin substrate without an intervention of another layer" (*id.* at 4).

The Examiner finds that Tanaka teaches this configuration. *Id.* at 5 (citing Tanaka FIG. 15). More specifically, the Examiner finds that conductor 84, which connects to via 82, has a second portion that is in direct physical contact with resin layer 150. *Id*. The Examiner determines that motivation existed to apply this teaching to Kikuchi so that Kikuchi's external electrode is in direct contact with the resin. *Id.*

We review the appealed rejections for error based upon the issues identified by Appellant, and in light of the arguments and evidence produced thereon. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential).

APPELLANT'S CONTENTIONS

Appellant first argues generally that the rejection fails to establish that the cited art discloses various limitations of claims 1 and 13. App. Br. 7–8. This general argument entails reproducing the last four limitations of claim 1's five limitations and emphasizing significant portions of the second, fourth and fifth limitations. *Id.* This lengthy assertion does not constitute an

argument on the merits, because "[a] statement [that] merely points out what a claim recites will not be considered an argument for separate patentability of the claim." 37 C.F.R. § 41.37(c)(1)(iv); *see In re Lovin*, 652 F.3d 1349, 1357 (Fed. Cir. 2011) (explaining that the applicable rules "require more substantive arguments in an appeal brief than a mere recitation of the claim elements and a naked assertion that the corresponding elements were not found in the prior art"). We, therefore, turn to Appellant's more specific arguments.

Appellant next points out that the present invention includes an electronic component (such as a semiconductor integrated circuit (IC)) embedded within a resin substrate (such as a circuit board) and that the electronic component includes two wiring layers: a first, uppermost wiring layer and a second wiring layer that is located under the first wiring layer. App. Br. 8. According to Appellant, the first, uppermost wiring layer includes a plurality of external electrodes, and one of these external electrodes is designated as a first external electrode. *Id.*

This first, external electrode, in turn, includes two sections: (1) a first section that has an upper surface contacting a via conductor that electrically connects the component's first external electrode to a wiring layer of the resin substrate, and (2) a second section that has a lower surface that contacts an internal via conductor that electrically connects the components external electrode to a second wiring layer. *Id.*

Appellant specifically notes that in the present invention, "the first wiring layer (e.g., an uppermost one of the chip wiring layers) of the semiconductor IC is <u>not covered</u> with an insulation layer of the semiconductor IC." *Id.* at 9. Appellant explains, "[a]s a result, when the

semiconductor IC is embedded in into the resin substrate, the first wiring layer of the semiconductor IC directly contacts the resin substrate, as defined in claims 1 and 13." *Id.* Appellant argues that "each of the references cited is silent about, and fails to teach or suggest[,] the above feature of the claimed invention." *Id.*

Addressing the references, Appellant first argues that Kikuchi does not teach exposing the whole uppermost wiring layer of the IC chip. *Id.* Appellant acknowledges that the Final Action cites to Figure 10B of Kikuchi, but argues that the combination of Kikuchi's Figures 10A and 11A reasonably evidences that "layer 210 is a first wiring structure that is located below the second wiring structure 220." App. Br. 9.

Appellant further argues that the uppermost wiring layer 222 of the second wiring structure 220 is covered with an insulation layer 221, and "[a]s a result, the second section cannot be in contact with the resin substrate, since the insulation layer 221 intervenes therebetween. *Id.* Appellant argues that "Hurwitz and Tanaka fail to make up the deficiencies of Kikuchi." *Id.*

Appellant also argues against the Examiner's separate rationale—that it would have been obvious to eliminate the insulation layer 221 of Kikuchi's second wiring structure 220 that covers the first wiring structure 210. *Id.* According to Appellant, such a modification would change structure and function as intended of Kikuchi. *Id.* Appellant argues that the references are unrelated, that they provide no motivation for such a modification, and that the Examiner's combination of the references is based upon impermissible hindsight. *Id.* at 10.

ANALYSIS

Appellant's arguments are unpersuasive. To be sure, the Examiner's reasoning arguably conflates three rationales for determining that the cited art renders claim 1 obvious. But any lack of clarity in the Final Action or Answer does not negate the three rationales' persuasiveness that the cited art renders these claims unpatentable. We address each rationale *seriatim* below to disambiguate the Examiner's rationales.

I.

The Examiner reasons, as follows:

> It would have been obvious to one having skill in the art at the effective filing date of the invention to modify Kikuchi's to[p] surface of the chip by letting the top wiring layer contact directly to the resin layer, as suggested by Tanaka, because the chip is embedded inside the circuit board, the resin layer can function as the top protection layer to protect the wiring on the surface of the chip.

Final Act. 5.

We understand the Examiner's position to be that Kikuchi's semiconductor chip 200 includes a semiconductor substrate 201, a first multilayer wiring structure 210 disposed on the top side of the substrate, and a second multilayer wiring structure 220 disposed on the first wiring structure 210. *E.g.* Kikuchi, FIGs. 10B, 11A. Kikuchi also discloses that this semiconductor chip 200 is disposed on a resin-type base insulating layer 101, the semiconductor chip is embedded in resin-based peripheral insulating layer 103, and the chip is covered by resin-based upper surface-side wiring structure 130. *E.g.*, *id.*, FIGs. 1, 2. The upper surface-side wiring structure 130 includes wiring lines 105a/b that are located immediately above the chip 200 and electrically connected to the uppermost

wiring layer 222 of the chip's second wiring structure 220 by means of vias 104. *E.g.*, *id.* FIGs. 1, 2, 9, 10A, 10B, 11A, 11B, ¶¶ 101–103.

We further understand the Examiner's position to be that Tanaka teaches that a semiconductor chip 20 is embedded in a resin circuit board 30, and a "conductor circuit" or external-electrode wiring trace 84 is disposed on top of the chip 20 so that the wiring trace's entire upper surface is exposed to a superposed resin layer 150 of the circuit board 30. Tanaka FIG. 15. Restated in the vernacular of claim 1, the upper surface of wiring trace 84 is "in contact with a resin layer included in [a superposed] resin substrate without an intervention of [another] layer."

We further understand the Examiner's position to be that (1) because Tanaka teaches that the top wiring layer of a semiconductor chip does not need to be covered with a dielectric layer in those situations where the chip subsequently is covered with a resin substrate, and (2) because Kikuchi's top wiring layer 222 of second wiring structure 220 will be covered with resin of the resin-based peripheral insulating layer 103, it would have been obvious to have omitted Kikuchi's top insulating layer 221 of the second wiring structure 220. We understand the Examiner's motivation for this modification to be that the insulating layer 221 would be unnecessary because the uppermost wiring layer 221 already will be covered and protected by resin of peripheral insulating layer 103. *See* Final Act. 5 ("because the chip is embedded inside the circuit board, the resin layer can function as the top protection layer to protect the wiring on the surface of the chip").

The Examiner thus provides a motivation for changing the structure of Kikuchi, which is not specifically addressed by Appellant. Appellant does

not provide persuasive arguments for why this rationale contains error or is otherwise improper.

II.

The rejection over the combination of Kikuchi and Tanaka also can be interpreted reasonably as proposing a second modification of the cited art. Specifically, the Examiner explains the following:

> Tanaka teaches, in figure 15, the second section (the portion of the conductor connecting to via 82) is in contact with a resin layer (resin layer 150) included in the resin substrate without an intervention of another layer (the second section directly connected to resin layer 150 of the circuit board).

Final Act. 5.

We understand the Examiner's second rationale to combine the references to be that Kikuchi's second wiring structure 220 of Figure 10A, for example, does not need to be modified so as to remove the uppermost insulating layer 221. Instead, Figure 15 of Tanaka may be relied upon to teach the details of how Kikuchi's uppermost wiring layer 222 can be interconnected to a superposed resin substrate, such as the resin substrate 130 that is depicted in Kikuchi's Figure 9. That is, Tanaka teaches the details for Kikuchi's vias 104. E.g. Kikuchi Figure 9.

More particularly, we understand the Examiner's second rationale to be that Kikuchi's uppermost insulating layer 221, as depicted in Figure 10A, is kept intact. Then the electrode-and-via structure 24/38/84 of Tanaka's Figure 15 may be added over Kikuchi's via hole 224, as depicted in Figure 10A, such that the entire upper surface of wiring trace 84 is exposed. Then Kikuchi's resin-based upper surface-side wiring structure layer 130 may be superposed over the second wiring structure 220 such that Kikuchi's wiring traces 105a/b of the resin structure 130 are electrically connected to

the wiring trace 84, just as the wiring trace 158 within the solder resist layer 70 of Tanaka's resin-based core substrate 30 is connected to chip trace 84 by means of via electrode 260. Tanaka, FIG. 15.

In such a combination, the upper surface of conductor circuit trace 84 would be in direct contact with a resin layer. *See* Tanaka, FIG. 15 (circuit board resin layer 150). We understand the motivation for such a combination to be to provide a functioning electrical connection between Kikuchi's semiconductor chip and a superposed resin board, as taught by the embodiment of Tanaka depicted in Figure 15. As the Examiner explains,

> Based on the teaching of Kikuchi and Tanaka, it [would have been] obvious to one having ordinary skill in the art to choose between two known configurations of the chip[,] such as having an insulating layer covering a portion of the top surface of the chip or not having an insulating layer on a portion of the top surface of the chip. The main purpose of the insulating layers in a circuit board is to prevent a short circuit between electronic components inside the circuit board. Choosing either configurations does not affect the function of the chip because the entire chip is already embedded and protected inside the insulating substrate of the circuit board.

Ans. 2–3.

The Examiner thus provides a motivation for changing the structure of Kikuchi, which is not specifically addressed by Appellant. Appellant does not provide persuasive arguments for why this rationale contains error or is otherwise improper.

III.

The rejection over the combined cited art also can be supported by a third interpretation. Specifically, the Examiner explains the following:

> Kikuchi suggests the whole wiring layer 21 being exposed on top surface of the semiconductor chip (figure 10B). Therefore, a

> portion of the wiring layer 21 is connected to via 104 [sic: 223], while the other portion of the wiring layer 21 is in contact with resin layer and internal via 23.[3]

Final Act. 5.

Furthermore, Kikuchi's Figure 10A depicts the second wiring structure 220 possessing a lowest most second insulating layer 221 that contacts the upper surface of the first wiring structure 210. And Figure 10B depicts the upper surface of the first wiring structure 210 having exposed wiring lines 21. As such, the combination of Figures 10A and 10B disclose the bottom surface of insulating layer 221 being in contact with the upper surface of wiring layer 21.

Kikuchi further discloses that the second insulating layers 221 of the second wiring structure 220 may be composed of a resin material. Kikuchi ¶ 164 ("[a]s the material of the second insulating layer [221], it is possible to suitably use a resin insulating material"), ¶ 174 ("a resin insulating material not containing a filler can be used as the second insulating layers in the second wiring structure layer 220"). As such, and because each of the following structures of Kikuchi include resin insulators, nothing in claim 1 reasonably limits the recited resin substrate from being interpreted as reading on the combination of Kikuchi's lower surface-side wiring structure layer 140, peripheral insulating structure 103, upper surface-side wiring structure 130, *and second wiring structure 220*, such as depicted in Kikuchi's Figures 9 and 10A.

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[3] Figures 10A and 11A of Kikuchi depict vias ***223*** of second wiring structure 220 making contact to the first wiring structure—not vias 104. Figure 1 depicts Kikuchi's vias 104 as making contact between the top of the chip 200 (which implies the top of the second wiring structure 220) and the overlying resin board 130.

Restated, under this third interpretation, Kikuchi, itself, without any modification by Tanaka's teachings, discloses the disputed limitation of "wherein the second section [(first wiring structure 210)] is in contact with a resin layer [(second wiring structure 220)] included in the resin substrate without an intervention of [another] layer." Note that in sustaining a multiple-reference rejection under 35 U.S.C. § 103(a), the Board may rely on fewer than all of the cited references without designating the affirmance as a new ground of rejection. *In re Boyer*, 363 F.2d 455, 458 n.2 (CCPA 1966) (citing *In re Bush*, 296 F.2d 491, 496 (CCPA 1961)).

Conclusions

For the listed reasons, Appellant has not persuaded us of error in the Examiner's obviousness rejection of independent claim 1. Accordingly, we sustain the Examiner's rejection of that claim, as well as independent claim 13, which recites similar claim language and for which Appellant presents similar arguments. App. Br. 7–14. We likewise affirm the obviousness rejections of dependent claims 2, 3, 5–8, 15, and 21–31, which Appellant does not argue separately. *Id.* at 14.

DECISION

The Examiner's decision rejecting claims 1–3, 5–8, 13, 15, and 21–31 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED