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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte REZA A. PAGAILA, BYUNG TAI DO, and LINDA PEI EE CHUA

Appeal 2018-002544
Application 13/225,683
Technology Center 2800

Before TERRY J. OWENS, CATHERINE Q. TIMM, and SHELDON M. MCGEE *Administrative Patent Judges*.

TIMM, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellants[2] appeal from the Examiner's decision to reject claims 51–72. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

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[1] In explaining our Decision, we cite to the Specification of September 6, 2011 ("Spec."), Final Office Action of December 15, 2016 ("Final Act."), Appeal Brief of May 10, 2017 ("Appeal Br."), Examiner's Answer of November 9, 2017 ("Ans."), and Reply Brief of January 9, 2018 ("Reply Br.").

[2] Appellants identify the real party in interest as STATS ChipPAC Pte. Ltd. Appeal Br. 1.

The claims are directed to a semiconductor device. *See, e.g.*, claims 51, 56, 62, and 68.

Figures 5a, 7a, 9a, and 11a are cross-sectional views of the device of the independent claims. We reproduce Figure 11a, as annotated by Appellants (Appeal Br. 12), to illustrate:

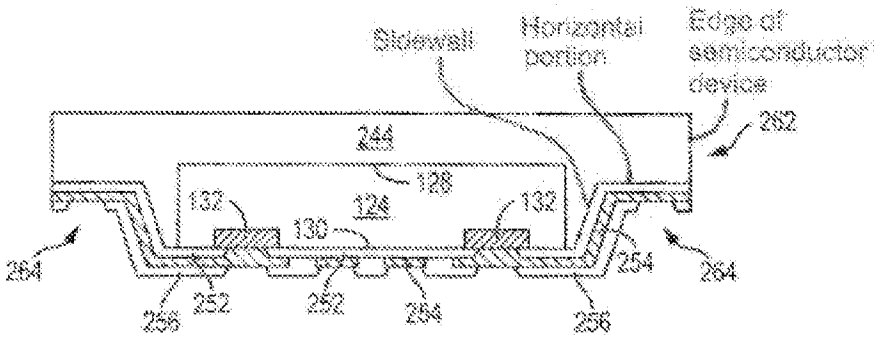
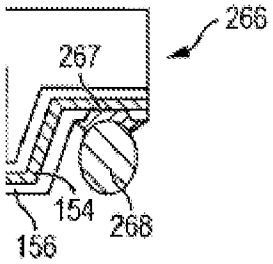


FIG. 11a

Annotated Figure 11a illustrates semiconductor device 262, which is a fan-out wafer level chip scale package (Fo-WLCSP)

The semiconductor device of Figure 11a includes encapsulant 244 deposited around semiconductor die 124. Spec. ¶ 72. As shown in annotated Figure 11a, encapsulant 244 extends outward from the side surfaces of semiconductor die 124 to form peripheral regions outside a footprint of semiconductor die 124. Spec. ¶ 72. The peripheral regions include recessed interconnect areas 264. *Id.*

The recess interconnect areas 264 reduce the profile of the semiconductor device 262. Spec. ¶ 72. This is because the interconnect structure (e.g., bumps 268 in Fig. 12 and bond wires 382 in Fig. 19) will fit within the recess interconnect areas as shown, for example, in Figure 12, which is reproduced below:



Portion of Figure 12 showing right-hand peripheral portion of semiconductor device 266 with bump 268 in recessed interconnect area 264 of Figure 11a

At recessed interconnect areas 264 (where bumps 268 reside), the encapsulant 244 includes a sidewall and a horizontal portion that extends from the sidewall to an edge of the semiconductor device 262. *See* Annotated Fig. 11a, above.

The semiconductor device 262 includes conductive layer (154 in Fig. 12, 254 in Fig. 11a), which is conformally applied over contact pads 132 and insulating layer 252 using a patterning and metal deposition process. Spec. ¶ 69. Conductive layer 254 electrically connects portions of the semiconductor die 124, such as the contact pads 132, to bumps (e.g. bumps 268 in Fig. 12) and bond wires (e.g., bond wires 382 in Fig. 19).

Claim 68 is the broadest claim on appeal and we reproduce this claim with reference numerals from Figure 11a to further illustrate:

> 68. A semiconductor device [262], comprising:
>
> a first semiconductor die [124];
>
> an encapsulant [244] deposited around side surfaces of the first semiconductor die [124] and including a recessed interconnect area [264] including a sidewall and horizontal portion of the encapsulant [264] in a peripheral region outside a footprint of the first semiconductor die [124], wherein the

> horizontal portion of the encapsulant [244] extends from the sidewall to an edge of the semiconductor device [262]; and
>
> a first conductive layer [254] formed over the first semiconductor die [124] and encapsulant [244] and extending from a contact pad [132] of the first semiconductor die [124] along the sidewall and over the horizontal portion of the encapsulant [244] within the recessed interconnect area [264].

Appeal Br. 44 (claims appendix).

The Examiner maintains the following rejections:[3]

A. The rejection of claims 54, 55, 60, 61, and 67 under 35 U.S.C. § 112 ¶ 1 as lacking written descriptive support;

B. The rejection of 62, 64, 66–68, 70, and 72 under 35 U.S.C. § 102(b) as anticipated by Meyer;[4]

C. The rejection of claims 65 and 71 under 35 U.S.C. § 103(a) as obvious over Meyer in view of Lee;[5]

D. The rejection of claims 51, 53, 55–58, 61, 63, and 69 under 35 U.S.C. § 103(a) as obvious over Meyer in view of Lin;[6]

E. The rejection of claims 52, 54, 59, and 60 under 35 U.S.C. § 103(a) as obvious over Meyer in view of Lin and Lee.

OPINION

[3] The Examiner withdrew the rejection of claims 51 and 56 under 35 U.S.C. § 112 ¶ 2. Ans. 2.
[4] Meyer et al., US 7,208,345 B2, issued April 24, 2007.
[5] Lee et al., US 2008/0137312 A1, published June 12, 2008.
[6] Lin et al., US 7,811,863 B1, issued October 12, 2010.

Rejection A

The Examiner rejects claims 54, 55, 60, 61, and 67 under 35 U.S.C. § 112 ¶ 1 as lacking written descriptive support. Final Act. 4–6. Because the issues are the same for claims 54 and 60, we address those claims together. Because the issues for claims 55, 61, and 67 are the same, we address those claims together.

Claims 54 and 60

For the rejection of claims 54 and 60, because claim 60 is broader than claim 54,[7] we select claim 60 as representative for discussing the issue on appeal.

Claim 60 depends from claim 56. Claim 56 requires a second conductive layer formed over the first semiconductor die. Although Appellants' label only one conductive layer 254, Figure 11b depicts conductive layer 254 as a pattern of conductive material leading from various parts of the semiconductor die 124 outward through the recessed interconnect areas 264 to the edge of the semiconductor device 262. Appellants annotate one portion of conductive layer 254 the first conductive layer and another portion of conductive layer 254 the second conductive

[7] Appellants direct their arguments to the narrower claim 54 and fail to argue claim 60 separately. Appeal Br. 10–13. This selection of narrower claims occurs throughout the Brief. Appellants also order their claims from narrowest independent claim (claim 51) to broadest independent claim (claim 68). Normally, claims are ordered in the opposite manner, i.e., from broadest to narrowest. *See* 37 C.F.R. § 1.75(g) and MPEP § 608.01(m) (9th ed. 2018) ("Claims should preferably be arranged in order of scope so that the first claim presented is the least restrictive."). Where error is identified in the rejection of broader claims, there is no need to separately consider the rejection of narrower claims. Thus, we select the broadest claims to begin our analysis in all cases.

layer.[8] Appeal Br. 11. We reproduce Appellants' annotated Figure 11b to show Appellants' labeling:

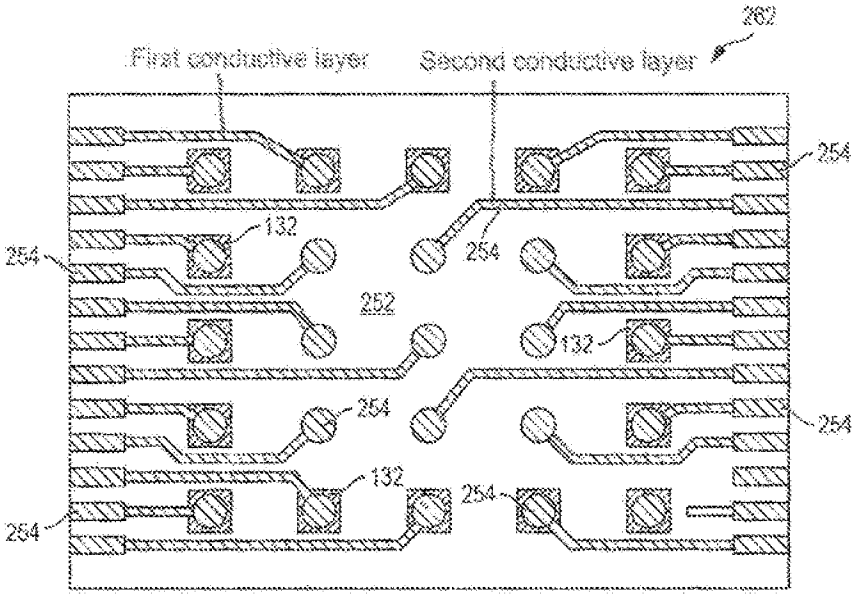


FIG. 11b

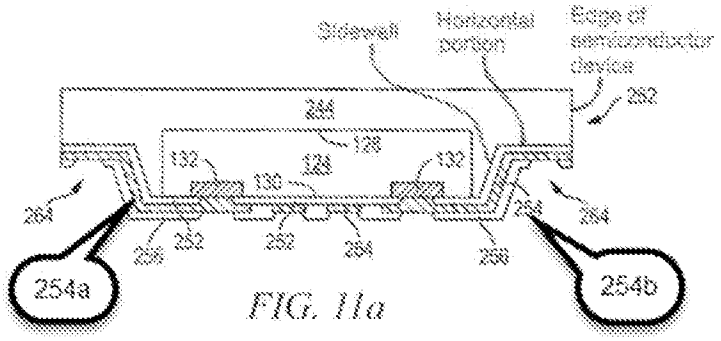
Annotated Figure 11b depicts a bottom view of the semiconductor device of Figure 11a

We will label the "first conductive layer" 254a and the "second conductive layer" 254b.[9] We reproduce an annotated Figure 11a to show the locations of two conductive layer portions 254a and 254b:

---

[8] What Appellant annotates as first and second conductive layers in Figure 11b are described in the written description as portions of conductive layer 254 electrically connected to contact pad 132 and other portions electrically common or electrically isolated depending on the design and function of semiconductor die 124. Spec. ¶ 69.

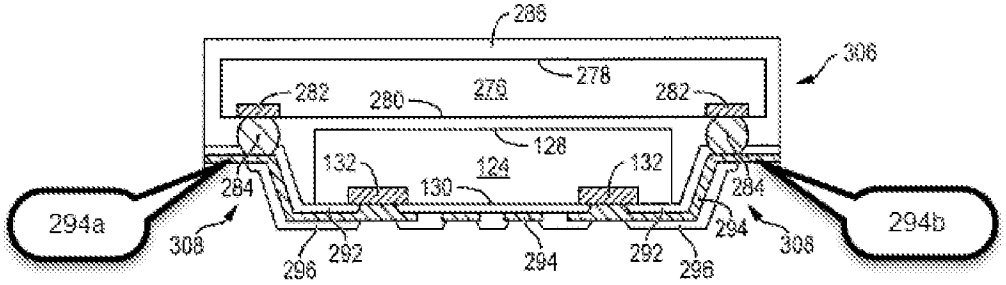
[9] As is evident from the need to annotate the drawings, the drawings fail to show details for a proper understanding of the claimed invention contrary to 37 C.F.R. § 1.83. *See* MPEP § 608.02(d) ("Any structural detail that is of sufficient importance to be described should be shown in the drawing."). The Examiner has objected to the drawings on other grounds.



Annotated Figure 11a illustrates a fan-out wafer level chip scale package (Fo-WLCSP) with first conductive layer portion 254a and second conductive layer portion 254b

Claim 60 further requires a second semiconductor die disposed within the first encapsulant over the first semiconductor die.

Figure 16 depicts a semiconductor device encompassed by claim 60. We reproduce Figure 16 with annotations to show the location of first and second conductive layer portions, which we label 294a and 294b:



Annotated Figure 16 depicts a Fo-WLCSP with recessed interconnect areas in a peripheral region of stacked semiconductor die

The device of Figure 16 includes second semiconductor die 276, which is added per the steps shown in Figures 15a–15e. Spec. ¶¶ 77–85.

Final Act. 2. However, Appellants should label all the annotated features reproduced in our Decision.

The steps of Figures 15a–15e are a continuation from the step shown in Figure 4e, which is a step in the process of forming the Fo-WLCSP semiconductor device of Figure 5a. Spec. ¶¶ 35, 77. Like the device of Figure 11a, the device of Figure 5a has separate portions of a conductive layer leading to various points on the semiconductor die to the areas for bonding to bumps or bond wires. *Compare* Fig. 5b, *with* Fig. 11b. Thus, like the conductive layer 254 depicted in Figure 11b, the conductive layer 294 of Figure 16 has first and second conductive layer portions. Claim 60 also requires a plurality of bumps. Annotated Fig. 16 at 284.

In rejecting claims 54 and 60, the Examiner finds that the Specification fails to disclose forming bumps between the second semiconductor die and the *second* conductive layer. Final Act. 4–6.

We agree with Appellants that when Figure 16 is read in the context of the entire written description, the structure recited in claims 54 and 60 has written descriptive support. Appeal Br. 10–11; Reply Br. 2–3. The key claim recitation, with reference numerals inserted, reads:

> a plurality of bumps [284] *formed between contact pads [282] of the second semiconductor die [276]* and the first conductive layer [294a] or *the second conductive layer* [294b] formed over the horizontal portion of the first encapsulant within the recessed interconnect area [308].

Appeal Br. 39, 41–42 (claims appendix) (emphasis added). As shown in Figure 16, the bumps 284 on the left side are formed between the left-hand contact pads 282 of second semiconductor die 276 and one conductive layer 294a (first conductive layer portion) and the bumps 284 on the right-hand side are formed between the right-hand contact pads 282 and another

conductive layer 294b (second conductive layer portion). Thus, Figure 16 and the written description provide the necessary support.

The true problem here is not one of lack of written descriptive support. The problem is that the drawings do not label the first and second conductive layer portions separately. The other problem is that the "first conductive layer" and "second conductive layer" language of the claims lacks antecedent basis in the written description and this has caused confusion.[10]

We do not sustain the Examiner's rejection of claims 54 and 60 as lacking written descriptive support.

Claims 55, 61, and 67

For the rejection of claims 55, 61, and 67 as lacking written descriptive support, we select claim 67 as representative to resolve the issues on appeal.

Claim 67 is directed to the embodiments shown in Figure 19 and 20. We reproduce the Examiner's annotated Figure 19 (Ans. 6), below:

[10] It would be appropriate for the Examiner to object to the written description under 37 C.F.R. § 1.75(d)(1) and require applicant to amend the description to provide antecedent basis for the terms appearing in the claims in a manner that does not add new matter. *See* MPEP § 608.01(o).

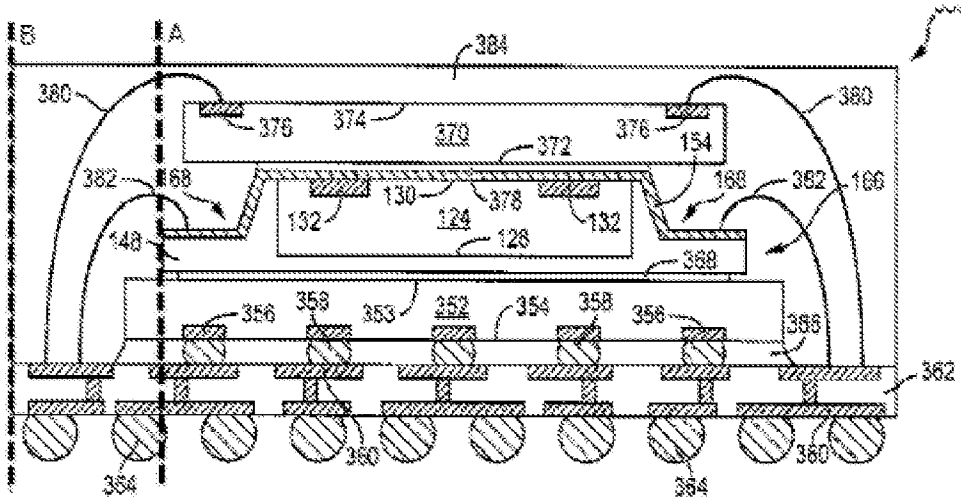


Figure 19 illustrates a Fo-WLCSP as an internal stacking module (ISM) in a package-in-package (PiP) arrangement

Claim 67 depends from claim 62. Claim 62 is directed to the structure in the center of Figure 19, i.e., the combination of semiconductor die 124, first encapsulant 148, and first conductive layer 154 with an interconnect structure (e.g., bond wires 382). Claim 67 further limits the semiconductor device to that of Figures 19 or 20 by adding "a substrate [362 in Fig. 19], wherein the first semiconductor die [124] is disposed over the substrate [362]" and "a second encapsulant [384] deposited over the substrate [362] and the interconnect structure [382] in the recessed interconnect area [168]. Claim 67, Spec. ¶ 104.

The Examiner finds that written descriptive support is lacking because claim 62 requires the first encapsulant 148 to have a horizontal portion extending from the sidewall *to an edge of the semiconductor device* and, in the embodiments of Figures 19 and 20, the edge of the semiconductor device is defined by the second encapsulant (dotted line B in annotated Figure 19),

which extends beyond the horizontal portion of the first encapsulant (dotted line A in annotated Figure 19). Final Act. 7; Ans. 6.

Appellants have not identified a reversible error in the Examiner's finding of lack of written descriptive support. Appellants contend that the edge of the semiconductor device remains the edge of semiconductor device 262 shown in Figure 11a (dotted line A in annotated Figure 19). Appeal Br. 12–13. Appellants are incorrectly reading the preamble of claim 67. The preamble of claim 67 designates the claim as directed to the semiconductor device that includes the structures recited in the body of claim 67. The body of claim 67 recites the second encapsulant 384 as included in this semiconductor device. The edge of the semiconductor device as shown in Figures 19 and 20 is not at the edge of the first encapsulant, but at the edge of the second encapsulant (dotted line B).

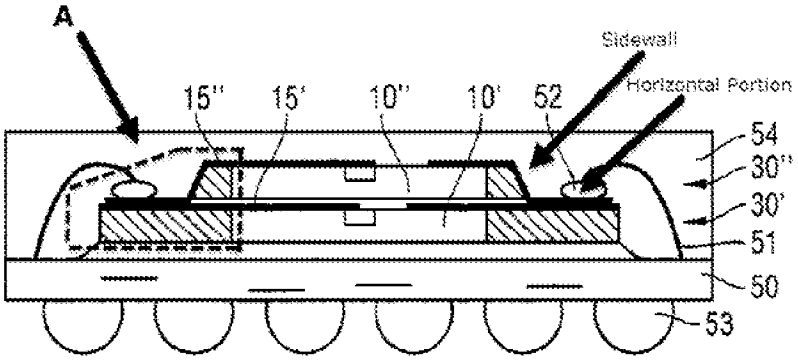
We sustain the Examiner's rejection of claims 55, 61, and 67 as lacking written descriptive support.

Rejection B

The Examiner rejects 62, 64, 66–68, 70, and 72 under 35 U.S.C. § 102(b) as anticipated by Meyer.

All of the rejected claims require an encapsulant including a recessed interconnect area including a sidewall and horizontal portion that extends from the sidewall. *See, e.g.*, claim 68.

The Examiner points to two different encapsulants shown in Meyer's Figure 19. Final Act. 10–11. We reproduce Figure 19, as annotated by the Examiner (Ans. 26), below:



Annotated Figure 19 depicts a semiconductor device including stacked ships 10' and 10"

We agree with Appellants that Meyer's stacked arrangement does not meet the requirements of the claims. Appeal Br. 33–34. Meyer's stacked arrangement is formed by placing embedded chip 30″ (die 10″ and mould 5″ (upper cross-hatched region adjacent die 10″ in Fig. 19)) onto adhesive layer 16′ (Fig. 12–13, col. 4, ll. 50–52), which is located on embedded chip 30′ (die 10′ and mould 5′ (lower cross-hatched region adjacent die 10′ in Fig. 19)). Meyer col. 4, ll. 50–68. The claims require "an encapsulant" having a sidewall and a horizontal portion. Meyer's two adhesively joined encapsulants are not "an encapsulant" with the necessary structure. Nor, contrary to the finding of the Examiner, is Meyer's conductive layer 15″ a first conductive layer extending over the horizontal portion of "the encapsulant," which must be read as the encapsulant defined in the first clause of claim 68, which has both a sidewall and a horizontal portion.

We do not sustain the Examiner's rejection of claims 62, 64, 66–68, 70, and 72 under 35 U.S.C. § 102(b) as anticipated by Meyer.

Rejections C–E

The Examiner rejects claims 65 and 71 under 35 U.S.C. § 103(a) as obvious over Meyer in view of Lee, claims 51, 53, 55–58, 61, 63, and 69 under 35 U.S.C. § 103(a) as obvious over Meyer in view of Lin, and claims 52, 54, 59, and 60 under 35 U.S.C. § 103(a) as obvious over Meyer in view of Lin and Lee. Each of these rejections relies on Meyer in the same capacity as in the anticipation rejection. The Examiner's application of Lin and Lee does not cure the defect discussed above.

We do not sustain the Examiner's rejection of claims 65 and 71 under 35 U.S.C. §103(a) as obvious over Meyer in view of Lee, claims 51, 53, 55–58, 61, 63, and 69 under 35 U.S.C. § 103(a) as obvious over Meyer in view of Lin, or claims 52, 54, 59, and 60 under 35 U.S.C. § 103(a) as obvious over Meyer in view of Lin and Lee.

CONCLUSION

In summary:

Claims Rejected	Basis	Reference(s)	Affirmed	Reversed
54, 60, 55, 61, 67	§ 112 ¶ 1		55, 61, 67	54, 60
62, 64, 66–68, 70, and 72	§ 102(b)	Meyer		62, 64, 66–68, 70, and 72
65, 71	§ 103(a)	Meyer, Lee		65, 71
51, 53, 55–58, 61, 63, and 69	§ 103(a)	Meyer, Lin		51, 53, 55–58, 61, 63, and 69
52, 54, 59, 60	§ 103(a)	Meyer, Lin, Lee		52, 54, 59, 60
Summary			55, 61, 67	51–54, 56–60, 62–66, 68–72

DECISION

The Examiner's decision is affirmed-in-part.

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

AFFIRMED-IN-PART