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Green, Howard, & Mughal LLP
5 Centerpointe Dr.
Suite 400
Lake Oswego, OR 97035

EXAMINER	
SHIN, JEFFREY M	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte AMR M. LOTFY, MOHAMED A ABDELSALAM, MOHAMMED W. EL MAHALAWY, NASSER A. KURD, and MOHAMED A. ABDELMONEUM

Appeal 2018-002046
Application 14/831,694
Technology Center 2800

Before LINDA M. GAUDETTE, MICHAEL P. COLAIANNI, and JEFFREY R. SNAY, *Administrative Patent Judges*.

SNAY, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision rejecting claims 38–47. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies Intel Corporation as the real party in interest. Appeal Br. 1.

BACKGROUND

The invention relates to a programmable digital phase locked loop which is said to be scalable across different manufacturing technologies. Spec. ¶ 16. Claims 38 and 42 read:

> 38. An apparatus comprising:
> an input supply node;
> an output supply node;
> a variable resistor coupled to the input supply node and to the output supply node; and
> a digital phase locked loop (PLL) including:
> a phase detector to detect a phase error between a reference signal and a feedback signal;
> a digital loop filter (DLF) to generate a digital code according to the phase error; and
> a digitally controlled oscillator (DCO) coupled to the output supply node, wherein the digital code is to adjust resistance of the variable resistor to modify an output supply provided by the output supply node.
>
> 42. An apparatus comprising:
> a digital loop filter (DLF) to generate a digital code according to a phase error;
> an input supply node;
> an output supply node;
> a variable resistor coupled to the input supply node and to the output supply node; and
> a digitally controlled oscillator (DCO) coupled to the output supply node, wherein the digital code is to adjust resistance of the variable resistor to modify an output supply provided by the output supply node.

Appeal Br. 16–17 (Claims Appendix). Each remaining claim on appeal depends from claim 38 or 42.

REJECTION

The Examiner maintains the rejection of claims 38–47 under 35 U.S.C. § 102(e) as unpatentable over Vandepas (US 2013/0249611 A1, published September 26, 2013).[2]

OPINION

The Examiner's rejection is provided at pages 3–5 of the Final Office Action. The Examiner finds that Vandepas describes a digital phase locked loop 101 having a digital controlled oscillator (106) which is driven by an output supply node (VccDCO). Final Act. 3 (citing Vandepas Fig. 1). Relevant to Appellant's arguments on appeal, the Examiner finds that Vandepas describes a variable resistor coupled to an input supply node (unregulated supply) and the output supply node (VccDCO), such that the output supply node (VccDCO) is adjusted by operation of the variable resistor in response to a digital code generated by the phase locked loop. *Id.* (citing Vandepas ¶¶ 35, 41, Fig. 2b).

Figures 1 and 2b from Vandepas are reproduced below.

[2] The Examiner's rejection of claims 24–27 and 48–52 is withdrawn. Ans. 4.

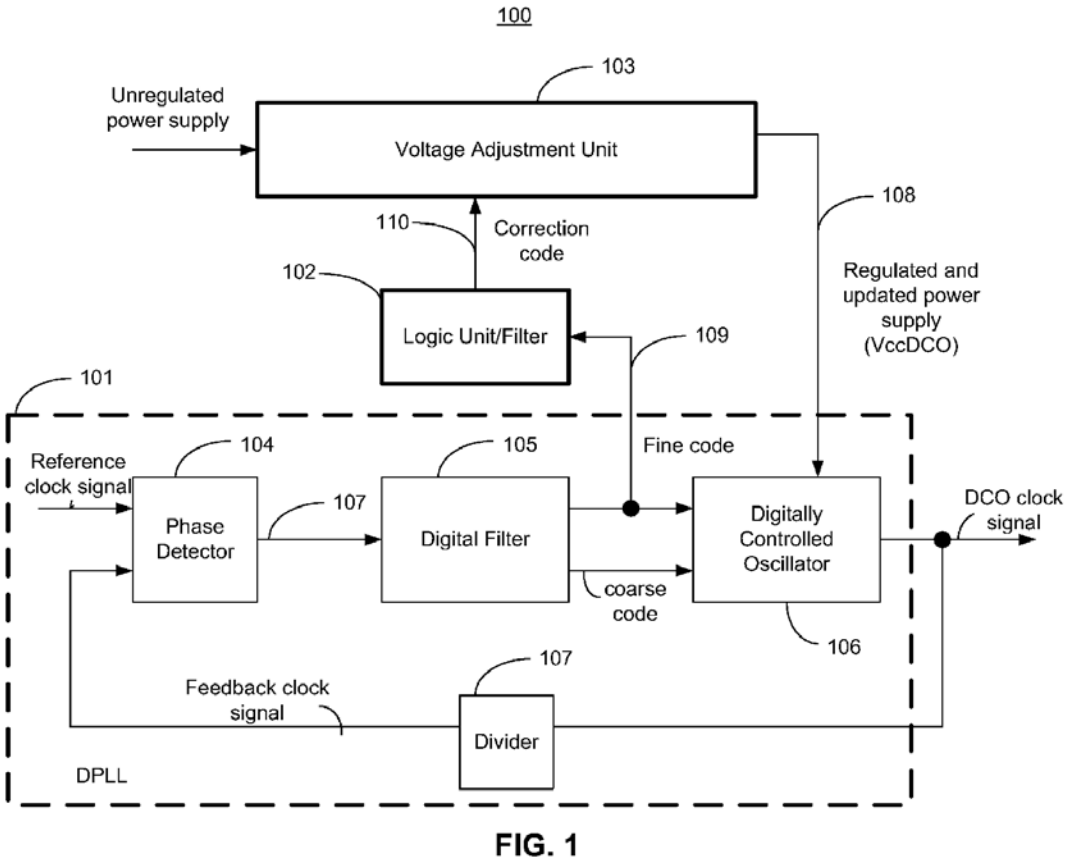

FIG. 1

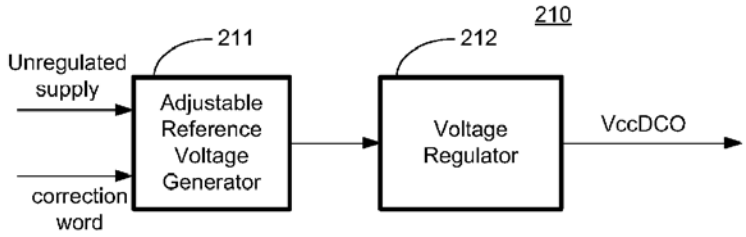

FIG. 2B

Figure 1 is a schematic drawing of a phase locked loop connected to a power supply having a voltage adjustment unit. Figure 2B is a schematic drawing of an embodiment of a voltage adjustment unit including an adjustable voltage generator.

Vandepas states that the voltage adjustment unit embodiment depicted in Figure 2B includes adjustable reference voltage generator 211. Vandepas ¶ 40. The Examiner finds that the adjustable reference voltage generator

includes a variable resistor in the form of a resistor divider network. Ans. 5 (citing Vandepas ¶ 41).

Appellant does not dispute that Vandepas describes a resistor divider network located and configured to adjust the unregulated input supply to yield a modified output supply provided by the output supply node. Appellant argues, however, that Vandepas does not disclose a variable resistor "coupled to the input supply node and to the output supply node." Appeal Br. 10. Rather, according to Appellant, Vandepas' resistor divider network "appears to be connected between a supply node and ground." *Id.* at 9. *See also* Reply Br. 8–9.

Appellant's argument is not persuasive of reversible error. There is no dispute that Vandepas describes a voltage adjustment unit coupled between an unregulated supply input node and a supply output node. *See* Vandepas Fig. 1. Nor does Appellant dispute that Vandepas describes an embodiment in which the above-noted adjustment unit includes a resistor divider network, which the Examiner characterizes as a variable resistor. Thus, regardless of whether a part of the described resistor divider network is connected to ground, a preponderance of the evidence supports the Examiner's finding that Vandepas describes a variable resistor (the voltage adjustment unit which includes a resistor divider network) coupled to input and output supply nodes.

Accordingly, the Examiner's rejection of claims 38–47 is sustained.

CONCLUSION

The Examiner's decision rejecting claims 38–47 is affirmed.

DECISION SUMMARY

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
38–47	102(e)	Vandepas	38–47	

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED