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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ANAND SESHADRI and THEODORE W. HOUSTON

Appeal 2018–001903
Application 13/196,042
Technology Center 2800

Before JEFFREY R. SNAY, BRIAN D. RANGE, and SHELDON M. McGEE, *Administrative Patent Judges*.

SNAY, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–8. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies Texas Instruments Incorporated as the real party interest. Appeal Br. 3.

BACKGROUND

The subject matter on appeal relates to static random access memory (SRAM) cells in an integrated circuit. Spec. ¶ 4. Claim 1 reads:

> 1. An integrated circuit, comprising:
>
> a SRAM cell array, said SRAM cell array containing SRAM cells, each said SRAM cell including:
>
> a Vdd node;
>
> a PMOS bit driver transistor, said bit driver transistor further including a gate node, a source node and a drain node; wherein said source node of said bit driver transistor is connected to said Vdd node;
>
> a bit-side data node; wherein said bit-side data node is connected to said drain node of said bit driver transistor;
>
> an NMOS bit load transistor, said bit load transistor further including a gate node, a source node and a drain node; wherein said drain node of said bit load transistor is connected to said bit-side data node;
>
> a Vss node; wherein said Vss node is connected to said source node of said bit load transistor;
>
> a PMOS bit-bar driver transistor, said bit-bar driver transistor further including a gate node, a source node and a drain node; wherein said source node of said bit-bar driver transistor is connected to said Vdd node and said gate node of said bit-bar driver transistor is connected to said bitside data node;
>
> a bit-bar-side data node; wherein said bit-bar-side data node is connected to said drain node of said bit-bar driver transistor, to said gate node of said bit driver transistor, and to said gate node of said bit load transistor;
>
> an NMOS bit-bar load transistor, said bit-bar load transistor further including a gate node, a source node and a drain node; wherein said drain node of said bit-bar load transistor is connected to said bit-bar-side data node, said source node of said bit-bar load transistor is connected to said Vss node, and said gate node of said bit-bar load transistor is connected to said bit-side data node;

> a PMOS bit passgate transistor, said bit passgate transistor further including a gate node, a first source/drain node and a second source/drain node; wherein said gate node of said bit passgate transistor is connected to a word line, said first source/drain node of said bit passgate transistor is connected to said bit-side data node, and said second source/drain node of said bit passgate transistor is connected to a bit data line;
>
> a PMOS bit-bar passgate transistor, said bit-bar passgate transistor further including a gate node, a first source/drain node and a second source/drain node; wherein said gate node of said bit-bar passgate transistor is connected to said word line, said first source/drain node of said bit-bar passgate transistor is connected to said bit-bar-side data node, and said second source/drain node of said bit-bar passgate transistor is connected to a bit-bar data line;
>
> a first n-well, wherein said first n-well contains said bit driver transistor; and
>
> a second n-well, wherein said second n-well contains said bit-bar passgate transistor;
>
> a data bus coupled to said SRAM cell array;
>
> an address bus coupled to said SRAM cell array;
>
> a data generation circuit coupled to said data bus and said address bus;
>
> a data usage circuit coupled to said data bus and said address bus; and
>
> an n-well bias control circuit coupled to said SRAM cell array, said n-well bias control circuit being configured to bias said first n-well and said second n-well independently.

Appeal Br. 26–28 (Claims Appendix).

Claim 4 recites an SRAM cell essentially as recited in claim 1. Each remaining claim on appeal depends from claim 1 or 4.

REJECTIONS

I. Claims 1–8 stand rejected under 35 U.S.C. § 112, second paragraph, as indefinite.

II. Claims 1–3 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Barth,[2] and Voelkel.[3]

III. Claims 4–8 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Barth, Voelkel, and Barbier.[4]

OPINION

Rejection I: indefiniteness

The Examiner determines each of claims 1–8 to be indefinite because, according to the Examiner, Appellant applies the terms "pull-up transistor" and "pull-down transistor" in a manner that is "inconsistent with well-established naming convention in the art." Non-Final Act. 4. Particularly, the Examiner points to the driver and load transistors described in the Specification, characterizes those transistors as so-called pull-up and pull-down transistors, and contends that such characterization is inconsistent with conventional terminology in which the pull-up transistor is known as a load transistor and the pull-down transistor is known as a driver transistor. *Id.* at 4–5.

Appellant argues that characterization of a transistor as "load" or "driver" is determined by whether it drives the bitline during Read. Appeal Br. 12. That is, the transistor driving the bitline during the Read operation is

[2] US 7,724,565 B2, issued May 25, 2010.
[3] US 2009/0154259 A1, issued June 18, 2009.
[4] US 7,307,873 B2, issued December 11, 2007.

the driver transistor, which may be a pull-up driver or a pull-down driver. *Id.* at 5.

A fundamental problem in the Examiner's reasoning is that the purportedly indefinite terms, "pull-up" and "pull-down," do not appear in Appellant's claims or Specification. Claim 1 recites, *inter alia*, driver transistors and load transistors, each with specified connections to other components of the claimed integrated circuit. The Examiner points to no ambiguity in those terms. To the contrary, the Examiner acknowledges paragraphs 17 and 18 of the Specification which provide definitions of both "driver transistor" and "load transistor." Non-Final Act. 4. The Examiner's apparent basis for the indefiniteness determination is that the described SRAM cell does not operate in the manner of conventional cells. Appellant acknowledges as much. *See* Appeal Br. 12 (explaining that, contrary to a conventional SRAM cell, "the inventive inverter of the Appellants' SRAM cell, the BL is driven (through the passgate) by the pull-up transistor in Read") (citing Spec. ¶ 46).

The fact that the recited transistors admittedly operate contrary to conventional SRAM cell transistors is not, alone, evidence of indefiniteness.

Rejection I is not sustained.

Rejections II and III: obviousness

Claim 1 requires, *inter alia*, a first n-well containing a bit driver transistor and a second n-well containing a bit-bar passgate transistor. Claim 4 includes that same recitation. A dispositive issue in this case is whether the combined disclosures of Barth and Voelkel support the Examiner's

determination that the above-mentioned n-well arrangement would have been obvious.[5]

The Examiner finds that Barth's Figure 2 depicts an SRAM cell 200 that includes a PMOS bit drive transistor (identified by the Examiner as the "left top PMOS" in Figure 2) and a PMOS bit-bar passgate transistor (P2 in Figure 2). Non-Final Act. 6. The Examiner finds that Barth is "silent with respect to n-well separation." *Id.* The Examiner further finds that Voelkel teaches a well separation and bias scheme, depicted in Voelkel's Figure 1, that includes "one or more N-wells to construct P-type transistor[s] and one or more P-wells to construct N-type transistors." *Id.* In light of these disclosures, the Examiner determines it would have been obvious to "apply the teaching of Voelkel to the teaching of Barth . . . such that an integrated circuit, as taught by Barth[], utilizes well separation, as taught by Voelkel." *Id.* at 7.

Appellant argues, *inter alia*, that Voelkel does not teach a first n-well that contains the bit driver transistor and a second n-well that contains the bit-bar passgate transistor. Appeal Br. 14. In response to Appellant's argument, the Examiner reasons that "Voelkel expressly teaches or suggests that *any* number of transistors can be placed in a particular well." Ans. 12. The Examiner does not identify in Voelkel any discussion of an association between a given n-well and a given transistor in an SRAM cell.

We are persuaded of reversible error in the Examiner's rejection of each of claims 1 and 4. The Examiner provides no reason why Voelkel's purported teaching that any number of transistors can be placed in a

[5] In rejecting claim 4, the Examiner additionally relies on Barbier in a manner unrelated to the recited n-well arrangement.

particular well would have provided a reason to particularly modify Barth's circuit to include a first n-well containing the recited bit driver transistor and a second n-well containing the recited bit-bar passgate transistor. That deficiency is exacerbated in the rejection of claims 2, 3, 5, and 6 which require particular additional transistors in each of the recited first and second n-wells. "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). For the foregoing reasons, we are persuaded that the Examiner has not met the burden of articulating sufficient reasoning to support the legal conclusion of obviousness.

Accordingly, Rejections II and III are not sustained.

CONCLUSION

The Examiner's decision rejecting claims 1–8 is reversed.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–8	112			1–8
1–3	103(a)	Barth, Voelkel		1–3
4–8	103(a)	Barth, Voelkel, Barbier		4–8
Overall Outcome				1–8

REVERSED