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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte HSIU-JEN LIN, CHUNG-SHI LIU, MING-DA CHENG, CHUN-CHENG LIN, YU-PENG TSAI, and CHENG-TING CHEN[1]

Appeal 2018-001621
Application 13/312,395
Technology Center 2800

Before DONNA M. PRAISS, CHRISTOPHER C. KENNEDY, and LILAN REN, *Administrative Patent Judges*.

Opinion for the Board by KENNEDY, *Administrative Patent Judge*.

Concurring Opinion by REN, *Administrative Patent Judge*.

KENNEDY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 1–5, 7–13, and 15–22. We have jurisdiction under 35 U.S.C. § 6(b). We AFFIRM.

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[1] According to the Appellants, the real party in interest is Taiwan Semiconductor Manufacturing Company, Ltd. App. Br. 3.

BACKGROUND

The subject matter on appeal relates to a solder bump process in integrated circuit manufacturing. *E.g.*, Spec. ¶ 1; Claim 1. Claim 1 is reproduced below from page 22 (Claims Appendix) of the Appeal Brief:

1. A method, comprising:

   performing a vacuum annealing on a substrate having at least one solder bump to reduce voids at an interface of the at least one solder bump, wherein the vacuum annealing is performed at a vacuum pressure ranging from 10^{-2} torr to 10^{-6} torr; and

   mounting a die over the substrate.

REJECTIONS ON APPEAL

The claims stand rejected under 35 U.S.C. § 103(a) as follows:

1. Claims 1, 2, 3, 7, 12, and 21 over Pendse '735 (US 2010/0178735 A1, published July 15, 2010) and Karasawa (US 5,877,079, issued Mar. 2, 1999);

2. Claims 4, 5, 13, 15–20, and 22[2] over Pendse '735, Karasawa, and Wang (US 2007/0207606 A1, published Sept. 6, 2007);

3. Claims 8–10 over Pendse '735, Karasawa, and Pendse '386 (US 2011/0084386 A1, published Apr. 14, 2011);

4. Claim 11 over Pendse '735, Karasawa, and Kitae (US 2009/0023245 A1, published Jan. 22, 2009).

[2] In the Final Rejection, the Examiner lists this as three separate grounds of rejection. *See* Final Act. 5–6 (first listing covering claims 4 and 5), 7 (second listing covering claims 13, 15, 16, and 22), 11 (third listing covering claims 17–20).

ANALYSIS

The Appellants argue the claims as a group and do not present distinct arguments for the separate grounds of rejection. We select claim 1 as representative of the appealed claims, and the remaining claims will stand or fall with claim 1.

After review of the cited evidence in the appeal record and the opposing positions of the Appellants and the Examiner, we determine that the Appellants have not identified reversible error in the Examiner's rejections. Accordingly, we affirm the stated rejections for reasons set forth below, in the Final Action, and in the Examiner's Answer. *See generally* Final Act. 2–17; Ans. 2–8.

The Examiner finds that Pendse '735 teaches each element of claim 1 except that it "fails to disclose vacuum annealing solder bumps 52 at 10^{-2} to 10^{-6} torr." Final Act. 3. The Examiner finds that Karasawa discloses a similar method in which vacuum annealing is performed on a substrate having at least one solder bump to reduce voids. *Id.* The Examiner acknowledges that Karasawa's disclosed pressure (0.02 torr, which is $2x10^{-2}$ torr) differs slightly from the claimed range but finds that the pressures are so close that one of ordinary skill in the art would have expected them to have the same properties. *Id.* at 3–4. Additionally, the Examiner finds that vacuum pressure "is a result effective variable for reducing voids in solder bumps." *Id.* The Examiner concludes that it would have been obvious "to have heated/annealed the solder bumps of Pendse at sub-torr vacuum pressure as taught by Karasawa et al. in order to remove or reduce voids formed in the solder bumps." *Id.* at 4.

The Appellants argue that the Examiner did not adequately establish that the pressure disclosed by Karasawa is "so close" to the claimed pressure that a person of ordinary skill in the art would have expected the pressures to yield the same results. App. Br. 8. In particular, the Appellants point out that the upper end of the claimed range is 0.01 torr, while Karasawa discloses a pressure of 0.02 torr, which is a 100% difference. *See* App. Br. 9. The Appellants also argue that the pressure in Karasawa increases after depressurization, that unexpected results support a conclusion of nonobviousness, and that the Examiner did not adequately establish that pressure is a result-effective variable. *Id.* at 9–15.

Those arguments do not persuade us of reversible error in the rejection. Both the Appellants' disclosure and Karasawa are directed to reducing voids in semiconductor devices. *Compare* Karasawa at Abstract, *with* Spec. ¶ 17. In its "Description of the Related Art," Karasawa recognizes that, "in a practical manufacturing process of a semiconductor device, a gas evacuation of a solder bump is performed in a relatively simple manner such as *annealing in a vacuum condition* or in an inert gas atmosphere, although it is recognized that such a method is not sufficient [to solve the issue of voids in solder bumps]." Karasawa at 2:46–53 (emphasis added). As part of its improved method, Karasawa teaches annealing under depressurized conditions followed by pressurizing the chamber "to a normal pressure while the temperature in the chamber" remains elevated. *Id.* at 8:29–67. Karasawa teaches that this method results in the "substantial[] eliminat[ion]" of voids in solder bumps:

> It was found that the void 4 in each of the solder bumps 1 was substantially eliminated (shrunk). It was recognized from the result that the void 4 can be substantially eliminated by melting

> the solder bump 1 under the depressurized condition; thereafter pressurizing the atmosphere while melted; and finally solidifying the solder bump 1.

Id. at 8:61–67.

We are not persuaded of reversible error in the Examiner's determination that 0.01 torr (the upper end of the claimed range) and 0.02 torr (the pressure disclosed in Karasawa's working examples) are close enough that a person of ordinary skill in the art would have expected them to have the same properties. *See In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003) ("[A] *prima facie* case of obviousness exists when the claimed range and the prior art range do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties."). The Appellants principally focus on the fact that, in *Titanium Metals Corp. v. Banner*, 778 F.2d 775 (Fed. Cir. 1985), the relevant difference was allegedly 10%, whereas here it is 100% (0.01 vs. 0.02). However, in absolute values (as opposed to percentages) the difference at issue here is 0.01 torr. Both 0.01 torr and 0.02 torr are low-pressure conditions, and, as the Examiner explains, the range recited by claim 1 actually covers several orders of magnitude (10^{-2} to 10^{-6}). *See* Ans. 2. Even acknowledging that the difference between 10^{-2} and 10^{-6} in absolute terms is "approximately 0.01 torr," *see* Reply Br. 2, that difference is comparable to the difference between the 0.02 torr of Karasawa and the 0.01 torr upper-end of the recited range.

We recognize that Karasawa indicates that the solder bumps may contain large voids after depressurization but prior to repressurization. *See* Karasawa at 7:18–52. However, the Appellants identify nothing in Karasawa that indicates what the size of the void would be absent

depressurization. The fact that repressurization may further shrink the void does not establish that Karasawa's depressurization conditions do not provide results the same as or similar to the depressurization conditions required by claim 1. Additionally, we observe that claim 1 does not exclude repressurizing subsequent to depressurizing. As the Examiner observes, "[n]either the present claims nor the specification specifies how the solder bumps are handled after the vacuum heating/annealing step, whereas Karasawa et al. provides detailed description for handling the solder bumps after the vacuum annealing step, i.e. the solder bumps are brought up to normal pressure to cool and solidify the solder bumps." Ans. 4. The end result of Karasawa's process involving vacuum annealing a solder bump at pressures that differ by the claimed pressures by as little as 0.01 torr is the "substantial[] eliminat[ion]" of voids. *See* Karasawa at 8:60–65. Accordingly, we are not persuaded of reversible error in the Examiner's determination that a person of ordinary skill in the art would have expected the same or similar results from 0.02 torr as from 0.01 torr.

Even were we to agree with the Appellants that 0.02 torr and 0.01 torr are not "close enough" to establish a prima facie case of obviousness, *see Peterson*, 315 F.3d at 1329, we also are not persuaded of reversible error in the Examiner's determination that pressure is a result-effective variable, which provides an independent basis for affirmance. In particular, Karasawa broadly discloses annealing under depressurized conditions, and Karasawa also observes that it is common in the art to anneal under vacuum conditions. *See, e.g.*, Karasawa at Abstract, 2:46–53. Although Karasawa provides working examples using a pressure of 0.02 torr, Karasawa discloses that the pressure during the vacuum annealing process is a variable that

affects void volumes. *See* Karasawa at 7:53–65 (providing the equation "V2=(P1/P2)xV1"). "A recognition in the prior art that a property is affected by the variable is sufficient to find the variable result-effective." *In re Applied Materials, Inc.*, 692 F.3d 1289, 1297 (Fed. Cir. 2012).

On this record, we are not persuaded by the Appellants' argument that pressure is not a result-effective variable. *See* App. Br. 13. In view of Karasawa's disclosures, a person of ordinary skill in the art would have understood that pressure is a result-effective variable and that depressurized/vacuum conditions are useful for reducing voids in solder bumps (even if combined with subsequent pressurization steps not excluded by claim 1), and a person of ordinary skill in the art would have been motivated to optimize pressures—including to pressures falling within the scope of claim 1, which differ from those explicitly disclosed by the prior art by only 0.01 torr—to achieve desired results. *See Applied Materials*, 692 F.3d at 1295 ("Discovery of an optimum value of a result effective variable . . . is ordinarily within the skill of the art.").

Finally, we are not persuaded that unexpected results are indicative of nonobviousness in this case. *See* App. Br. 10–13. The burden of establishing that unexpected results support a conclusion of nonobviousness rests with the Appellants. *In re Huang*, 100 F.3d 135, 139 (Fed. Cir. 1996). The Appellants have not carried that burden.

"[W]hen unexpected results are used as evidence of nonobviousness, the results must be shown to be unexpected compared with the closest prior art." *In re Baxter Travenol Labs.*, 952 F.2d 388, 392 (Fed. Cir. 1991). "[I]t is not enough to show that results are obtained which differ from those obtained in the prior art: that difference must be shown to be an *unexpected*

difference." *In re Klosak*, 455 F.2d 1077, 1080 (CCPA 1972) (emphasis in original). Here, the Appellants argue that because Karasawa's solder bumps may contain a void after the depressurizing step, it is unexpected that the Appellants' own process "results in a reduction of a void." App. Br. 10–11. However, the Appellants provide no evidence of what the size of Karasawa's voids would have been absent a depressurization step. Additionally, and as observed above, Karasawa expressly recognizes that prior art methods annealed under vacuum conditions. Although Karasawa states that annealing under vacuum conditions "is not sufficient" to fully solve the issue of voids, the implication is that annealing under vacuum conditions or in an inert gas atmosphere at least ameliorates the problem to some extent. *See* Karasawa at 2:46–53. Thus, the evidence of record supports a finding that a person of ordinary skill in the art would have expected vacuum annealing to yield desirable results with respect to the issue of voids in solder bumps. On this record, we are not persuaded by the Appellants' unexpected results argument.

In summary, we have carefully considered the Appellants' arguments, and we are not persuaded of reversible error in the Examiner's rejection of claim 1. *See In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011) ("[I]t has long been the Board's practice to require an applicant to identify the alleged error in the examiner's rejections . . . .").

CONCLUSION

We AFFIRM the Examiner's rejections of claims 1–5, 7–13, and 15–22.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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REN, *Administrative Patent Judge*, concurring.

I respectfully concur in only the judgment to hold claims 1–5, 7–13, and 15–22 unpatentable in view of the prior art.