UNITED STATES PATENT AND TRADEMARK OFFICE

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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Ex parte JONGHYUN LEE, YUNRUI LI,
MAHESH BABURAO GIRKAR, and
AMRISH SRIVASTAVA

———————————

Appeal 2018-001590
Application 14/270,117[1]
Technology Center 2100

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Before ERIC S. FRAHM, DENISE M. POTHIER, and
CARL L. SILVERMAN, *Administrative Patent Judges.*

FRAHM, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's final
rejection of claims 1–20, which are all the claims pending in this application.
We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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[1] According to Appellants, the real party in interest is Oracle International
Corporation. App. Br. 1.

Appellants' Invention

Appellants' application relates to "databases, and more specifically, to checkpoints for databases during media recovery." Spec. ¶ 1. Media recovery, or backups, for databases "are generally scheduled periodically, with change records recorded for any database changes that occur between the backups," and "[t]he performance of the media recovery may thus have a direct impact on query latency and database availability." Spec. ¶ 2. "Periodic checkpointing may be used to safeguard the media recovery process, allowing the media recovery process to resume from the last checkpoint rather than from the backup files after a failure occurs." Spec. ¶ 4. Appellants' invention provides a more "efficient and high performance checkpointing for databases during media recovery." Spec. ¶ 7. Claim 1, reproduced below with bracketed material and emphases added, is illustrative of the claimed subject matter:

> 1. A method comprising:
> applying, for a standby database, a plurality of change records received from a primary database, the applying creating one or more queues of dirty buffers, each dirty buffer having a logical time of a change record that was applied into said dirty buffer;
> maintaining a mapping for a plurality of system clock timestamps, wherein each system clock timestamp of said plurality of system clock timestamps is mapped to a logical time of a particular change record of said plurality of change records, said particular change record being a latest applied change record for the standby database as of the logical time that corresponds to said each system clock timestamp;
> [A.] *using the mapping, determining a target logical time mapped to a target system clock timestamp that is prior to a present system clock timestamp by at least a checkpoint delay;*
> [B.] *creating a checkpoint describing one or more database files of the standby database at a consistent logical*

*time, wherein the creating writes a set of dirty buffers, from
the one or more queues of dirty buffers, that have logical times
up to the target logical time;*
     wherein the method is performed by one or more
computing devices.

The Examiner's Rejections

(1) The Examiner rejected claims 1, 8, and 14 under 35 U.S.C.
§ 112(b) as being indefinite for failing to particularly point out and distinctly
claim the subject matter which Appellants regard as the invention, namely
the clause "maintaining a mapping . . . said particular change record being a
latest applied change record . . . each . . . timestamp" recited in each of
independent claims 1, 8, and 14. Final Act. 10. This rejection has been
withdrawn by the Examiner (Ans. 2), and is, therefore, not before us on
appeal. Accordingly, we do not address Appellants' arguments (App. Br.
6–10) in this regard herein.

(2) Claims 1–20 stand rejected under 35 U.S.C. § 101 as being
directed to patent-ineligible subject matter. Final Act. 11–14. That is, the
claims are directed to patent ineligible subject matter because the claimed
invention is directed to a judicial exception (i.e., a law of nature, a natural
phenomenon, or an abstract idea) without significantly more. Specifically,
the Examiner determines that claims 1–20 are drawn to the abstract idea of
creating queues of dirty buffers and creating checkpoints for database files.
Final Act. 12; Ans. 4–11. For purposes of analysis below, claim 1 is
illustrative.[2]

_____

[2] Appellants present arguments as to the eligibility of claims 1, 8, and 14
(App. Br. 10), primarily addressing claim 1 (*see* App. Br. 10–18; Reply Br.
6–13). Independent claims 8 and 14 recited commensurate limitations as

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(3) Claims 1–20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamura (US 2006/0010180 A1; publ. Jan. 12, 2006) and Diaconu (US 2014/0172803 A1; publ. June 19, 2014). Final Act. 15–20; Ans. 15–19.

Issues on Appeal

(1) Did the Examiner err in rejecting claims 1–20 as being directed to patent-ineligible subject matter?

(2) Did the Examiner err in rejecting claims 1–20 as being obvious because the combination of Kawamura and Diaconu fails to teach or suggest the checkpointing method, including limitations [A.] and [B.], as set forth in independent claim 1 *supra*, and as commensurately set forth in remaining independent claims 8 and 14?

ANALYSIS

We have reviewed the Examiner's rejections (Final Act. 11–20) in light of Appellants' arguments that the Examiner has erred (App. Br. 10–21; Reply Br. 2–13), in light of the Examiner's response to Appellants' arguments in the Appeal Brief (Ans. 2–19). We agree with Appellants' arguments as to both and eligibility and obviousness issues.

Section 101 — Patent Eligibility

Eligibility under 35 U.S.C. § 101 is determined using the *Alice/Mayo* framework. *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 134 S. Ct. 2347 (2014).

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limitations [A.] and [B.] of claim 1. Therefore, the below discussion of claim 1 is determinative of our outcome related to the § 101 rejection for all claims. Except for our ultimate decision, we do not discuss claims 2–20 further.

The first step involves determining whether the claims at issue are directed to a patent-ineligible concept. *Id*. at 2355. The second step involves determining whether the elements of the claim contain an inventive concept sufficient to transform a claimed abstract idea into a patent-eligible application. *Id*. at 2357. The "inventive concept" may arise in one or more of the individual claim limitations or in the ordered combination of the limitations. *Alice*, 134 S. Ct. at 2355 (internal quotation marks and citation omitted).

In *Bascom*, the Federal Circuit deferred consideration of the specific claim limitations' narrowing effect for *Alice* step two. *BASCOM Global Internet Servs., Inc. v. AT&T Mobility LLC*, 827 F.3d 1341, 1349 (Fed. Cir. 2016). The Federal Circuit held that determining whether the claimed inventive concept is a technical improvement can aid in evaluating the second step in the *Alice/Mayo* framework:

> The district court thus concluded [wrongly] that BASCOM had not asserted adequately that the claims disclose an inventive concept because the limitations, "considered individually, or as an ordered combination, are no more than routine additional steps involving generic computer components and the Internet, which interact in well-known ways to accomplish the abstract idea of filtering Internet content." [*District Court Order*, 107 F. Supp.3d at 655.]

> We agree with the district court that the limitations of the claims, taken individually, recite generic computer, network and Internet components, none of which is inventive by itself. BASCOM does not assert that it invented local computers, ISP servers, networks, network accounts, or filtering. Nor does the specification describe those elements as inventive.

> However, we disagree with the district court's analysis of the ordered combination of limitations. . . . As is the case here, an

> inventive concept can be found in the non-conventional and non-generic arrangement of known, conventional pieces.
>
> . . . .
>
> . . . . [T]he patent *describes how its particular arrangement of elements is a technical improvement* over prior art ways of filtering such content.

Bascom, 827 F.3d at 1349–50 (bracketed matter and emphasis added).

Alice/Mayo — Step 1

The Examiner finds claims 1–20 are patent-ineligible because independent claim 1 is directed toward the abstract ideas of (i) a "data structure having one or more queues of dirty buffers, checkpoints for databases" (Final Act. 12); (ii) "creating queues of dirty buffers, creating checkpoint[s] for database files" (*id.*); and (iii) "collecting, manipulating data" (Ans. 4; *see also* Ans. 9).

Instead of using a definition of an abstract idea, "the decisional mechanism courts now apply is to examine earlier cases in which a similar or parallel descriptive nature can be seen—what prior cases were about, and which way they were decided." *Amdocs (Isr.) Ltd. v. Openet Telecom, Inc.*, 841 F.3d 1288, 1294 (Fed. Cir. 2016) (citing *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353–54 (Fed. Cir. 2016)); *accord* United States Patent and Trademark Office, JULY 2015 UPDATE: SUBJECT MATTER ELIGIBILITY, 1–11 (July 30, 2015), https://www.uspto.gov/sites/default/files/documents/ieg-july-2015-update.pdf (instructing Examiners that "a claimed concept is not identified as an abstract idea unless it is similar to at least one concept that the courts have identified as an abstract idea") (*id.* at 3). As part of this inquiry, we must "look at the 'focus of the claimed advance over the prior art' to determine if the claim's 'character as a whole' is directed to

excluded subject matter." *Affinity Labs of Tex., LLC v. DirecTV, LLC*, 838 F.3d 1253, 1257–58 (Fed. Cir. 2016) (internal citations omitted).

Here, Appellants' claims are directed not only to (i) collecting and manipulating data; and (ii) creating queues of dirty buffers and checkpoints for database files, but to using a mapping to determine a target logical time mapped to a target system clock timestamp that is prior to a present system clock timestamp by at least a checkpoint delay (limitation [A.] recited in claim 1, and commensurately recited in claims 8 and 14), and then creating a checkpoint at a consistent logical time by writing a set of dirty buffers having logical times up to the target logical time (limitation [B.] recited in claim 1, and commensurately recited in claims 8 and 14). Appellants disclose in the Specification that using the mapping to determine a logical time stamp, which in turn allows the creation of incremental checkpoints based on an adjustable delay, "allows the checkpointing process to be load balanced over time, keeping the standby database responsive for other processes, such as a read-only standby database" (Spec. ¶ 19; *see also* ¶¶ 63–69 (discussing creating checkpoint 194 at a consistent logical time) and ¶¶ 73–75 (adjusting checkpoint time delay 192 for efficient operation)). And, claims 1, 8, and 14 each recite using a mapping to determine a target logical time based on a checkpoint delay, which in turn allows the creation of incremental checkpoints based on the adjustable delay. In this light, we agree with Appellants' contentions (App. Br. 16–17; Reply Br. 6–8) that claims 1, 8, and 14 are directed to technical improvements in computer

performance by load balancing in order to improve the quality and reliability, and, thus, claims 1, 8, and 14 are patent-eligible.

And, although the Examiner states in the Answer that the subject matter of claims 1, 8, and 14 "is not meaningfully different than those performing checkpoints for databases found by the courts to be abstract idea[s]" (Final Act. 12), we agree instead with Appellants that "the subject matter eligibility of checkpoints for databases has not been decided by the courts or categorically by the Office" (App. Br. 16). The Examiner has not pointed to, and we are not aware of, any binding case that determined the eligibility of *checkpointing* for databases.

Finally, we agree with Appellants (Reply Br. 9–11) that the Examiner's reliance on *Electric Power Group, LLC v. Alstom SA*, 830 F.3d 1350 (Fed. Cir. 2016), *Intellectual Ventures I LLC v. Capital One Bank*, 792 F.3d 1363 (Fed. Cir. 2015), and *Content Extraction and Trans. v. Wells Fargo Bank*, 776. F.3d 1343 (Fed. Cir. 2014) is misplaced because the claims at issue in these cases differ from claims 1, 8, and 14 before us in the instant case on appeal (which are directed to computer-functionality improvements as previously explained).

Alice/Mayo — Step 2

In the event that the claims are considered to be directed to an abstract idea, we turn to step 2. The Examiner finds the claims "do not include additional elements that are sufficient to amount to significantly more than the judicial exception because the additional elements when considered both individually and as an ordered combination do not amount to significantly more than the abstract idea" (Final Act. 12; *see also* Ans. 7).

The Examiner determines the method of claim 1 (i) is performed by the computing device using generic computer components (*e.g.*, a database and/or database structure) to perform routine and conventional activities such as to create and/or write dirty buffers from queues (Final Act. 12–13); and (ii) "merely describe[s] the 'creating checkpoint' function of the abstract idea itself, without particularity" (Ans. 7). The Examiner, thus, determines the recited steps/elements recited in claim 1, taken individually or as an ordered combination, (i) "recite no more than routine steps of 'using the mapping [. . .]';[']creating a checkpoint [. . .]', using generic database computer and conventional database processing activities" (Ans. 7); and (ii) "neither improve the functions of the database computer itself, nor provide specific 'checkpoint' or meaningful guidance for implementing the abstract concept" (*id.*).

The Examiner also determines that determining a logical time and creating a checkpoint as recited in claim 1 "aris[es] in the realm of computer database technology" (Ans. 11), "recite merely generic 'creating a checkpoint' in [a] database" (Ans. 7), and "when considered as an arrangement, do not provide a significant improvement to existing technological processes" (Ans. 11).

Although the recited dirty buffers, queues, and database limitations recited in claim 1 may be conventional and routine in the computer arts (*see Mortgage Grader Inc. v. First Choice Loan Servs., Inc.*, 811 F.3d 1314, 1324–25 (Fed. Cir. 2016) (noting that components such an "interface," "network," and "database" are generic computer components that do not satisfy the inventive concept requirement)), as an ordered combination the recited steps/elements in the claims *do* amount to significantly more.

Specifically, we are persuaded by Appellants' arguments (App. Br. 18–20; Reply Br. 11–13) that the steps of (i) using a mapping to determine a target logical time, and (ii) creating incremental checkpoints using adjusted delays, the created checkpoints involving writing dirty buffers, having logical times up to the determined target logical time, from queue(s) render claims 1, 8, and 14 recite significantly more than the abstract idea of simply creating checkpoints for databases.

Additionally, as to claim 1 steps [A.] and [B.], we disagree with the Examiner's conclusion that these steps are routine and conventional. These steps recite specific limitations that require the Examiner to undertake a more specific analysis to show they are routine and conventional. We do not find such specific analysis in the rejection on appeal. *See, e.g.,* Ans. 7, 9, 11. That is, we conclude the Examiner has provided insufficient analysis or support to show steps [A.] and [B.] are routine and conventional. Therefore, there is insufficient support in the record, for a conclusion that the detailed functions and elements of the claimed invention do not transform the abstract idea into eligible subject matter. As our reviewing court noted in *McRO, Inc. v. Bandai Namco Games Am. Inc.*, 837 F.3d 1299 (Fed. Cir. 2016), it is important to determine "whether the claims . . . focus on a specific means or method that improves the relevant technology or are instead directed to a result or effect that itself is the abstract idea and merely invoke generic processes and machinery." *Id.* at 1314. In other words, a claim that defines the way by which a computer-related result is achieved is distinguishable from a patent-ineligible claim that simply describes a result. Here, the specific limitations of claims 1, 8, and 14 provide a way of achieving improved checkpointing for a standby database using time

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mapping, resulting in load balancing. Accordingly, claims 1, 8, and 14 are directed to "a specific means or method that improves the relevant technology" and not simply "a result or effect that itself is the abstract idea." *Id.*

Summary

We, therefore, find independent claim 1 is not directed to an abstract idea. And, even assuming claim 1 was drawn to an abstract idea, we find claim 1 also contains an inventive concept, and recites a technical improvement, sufficient to transform the claimed abstract idea into a patent-eligible application. Accordingly, claim 1 is drawn to patent eligible subject matter. As indicated previously, independent claims 8 and 14, as well as dependent claims 2–7, 9–13, and 15–20, are similar in scope to claim 1. Accordingly, for similar reasons to those discussed above, we find the Examiner erred in finding claims 1–20 to be patent-ineligible.

Obviousness

The Examiner finds Kawamura teaches all of the recited method steps recited in claim 1, except for the limitation "'a plurality of timestamps with respect to change of records'" (Final Act. 17), and relies on Diaconu as disclosing "'a plurality of timestamps with respect to change of records'" (*id.*). *See* Final Act. 16–18. The Examiner finds the combination of Kawamura and Diaconu discloses all the limitations of independent claim 1, including that Kawamura teaches (i) using a mapping to determine a target logical time as recited in limitation [A.] (Final Act. 17 (citing Kawamura ¶¶ 77, 80–82)); and (ii) creating a checkpoint by writing dirty buffers having logical times up to the target logical time as recited in limitation [B.] (Final Act. 17 (citing Kawamura ¶¶ 80–84)). *See* Final Act. 16–17; Ans. 2–6.

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Appellants contend, among other things, that Kawamura fails to teach
limitation [A.] and limitation [B.]. *See* App. Br. 10–14. We are persuaded
by Appellants' arguments.

Limitation [A.] of claim 1 recites:

> using the mapping, determining a target logical time
> mapped to a target system clock timestamp that is prior to a
> present system clock timestamp by at least a checkpoint delay.

Limitation [B.] of claim 1 recites:

> creating a checkpoint describing one or more database
> files of the standby database at a consistent logical time, wherein
> the creating writes a set of dirty buffers, from the one or more
> queues of dirty buffers, that have logical times up to the target
> logical time.

Kawamura discloses (i) a disaster recovery method utilizing a
checkpoint processing section 112 to transmit status/log information
(Kawamura Title; Abstr.; ¶¶ 45, 65, 81, 82; Fig. 6); and (ii) using mapping
tables 15 and 35 indicating log and status information (Kawamura ¶¶ 75, 77,
79). However, Kawamura is silent as to creating checkpoints by writing
dirty buffers from queues *having logical times up to a target logical time*, as
set forth in limitation [B.], and doing so using a mapping to determine a
target logical time mapped according to a checkpoint delay, as set forth in
limitation [A.].

Specifically, paragraphs 80–84 of Kawamura, relied on by the
Examiner as teaching this limitation, merely disclose "checkpoint
acquisition" (¶ 81), wherein checkpoint processing section 112 "stores status
information indicating the location of the log record *at that time*"

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(¶ 81) (emphasis added), and processes "the status information indicating the location of the log record that is *the latest at that time point*" (¶ 82) (emphasis added).

We agree with Appellants that the recited "target logical time is historical, not current, because Claim 1 recites 'a checkpoint delay'" (App. Br. 10). As a result, we agree with Appellants that "Kawamura does not disclose creating a checkpoint . . . [wherein the creating] writes dirty buffers that have logical times up to the target logical time, as Claim 1 specifies" (App. Br. 11). Finally, we also agree with Appellants' contentions (App. Br. 11–12) that Kawamura only indicates a storage location of log records, and does not disclose each dirty buffer having a logical time.

In view of the foregoing, we are constrained by the record to find the Examiner erred in rejecting independent claim 1, independent claims 8 and 14, which recite commensurate limitations, and respective dependent claims 2–7, 9–13, and 15–20 for the same reasons.

CONCLUSIONS

(1) Appellants have established that the Examiner erred in rejecting claims 1–20 under 35 U.S.C. § 101 as being directed to patent-ineligible subject matter.

(2) The Examiner erred in rejecting claims 1–20 as being obvious because the combination of Kawamura and Diaconu fails to teach or suggest the checkpointing method, including limitations [A.] and [B.], as set forth in independent claim 1 *supra,* and as commensurately set forth in remaining independent claims 8 and 14.

(3) On this record, claims 1–20 have not been shown to be unpatentable.

DECISION

We reverse the Examiner's decision to reject claims 1–20.

REVERSED