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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte RAJAT CHAUHAN and KEITH E. KUNZ

Appeal 2018-001574
Application 14/951,877
Technology Center 2800

Before JEFFREY T. SMITH, JAMES C. HOUSEL, and
N. WHITNEY WILSON, *Administrative Patent Judges*.

HOUSEL, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

Appellant[2] appeals under 35 U.S.C. § 134(a) from the Examiner's decision finally rejecting claims 1–9 and 18–27 under 35 U.S.C. 103 as unpatentable over Eimitsu[3] in view of Inoue,[4] Ho,[5] and Kalb,[6] adding

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[1] Our decision refers to the Specification ("Spec.") filed November 25, 2015, the Examiner's Final Office Action ("Final Act.") dated February 14, 2017, Appellant's Appeal Brief ("Appeal Br.") filed July 31, 2017, and the Examiner's Answer ("Ans.") dated August 31, 2017.
[2] Appellant is the Applicant, Texas Instruments Incorporated, which is identified in the Appeal Brief as the real party in interest (Appeal Br. 1).
[3] Eimitsu et al., US 7,443,207 B2, issued October 28, 2008 ("Eimitsu").
[4] Inoue, US 2013/0120025 A1, published May 16, 2013 ("Inoue").
[5] Ho et al., US 7,893,726 B1, issued February 22, 2011 ("Ho").
[6] Kalb, US 2005/0218980 A1, published October 6, 2005 ("Kalb").

AAPA[7] to cover claim 10. We have jurisdiction over the appeal. 35 U.S.C. § 6(b).

We AFFIRM.

STATEMENT OF THE CASE

The invention relates to an ultralow power reduced coupling clocked comparator or sense amp flip flop (Title; Spec. ¶ 3). As the Inventors disclose, a clocked comparator receives an input signal, a reference signal, and a clock signal, and compares the input signal to the reference signal on a clock transition (*id.* ¶ 4). The comparator output signal then transitions to a state indicating whether the input signal exceeds the reference signal (*id.*). In general, a comparator includes symmetric left and right sides of transistors that receive the respective input and reference signals and, in response to a clock signal, couples signals from each side to a latch stage (*id.* ¶¶ 5, 8). A precharge phase for the comparator occurs when the clock signal is low, and a regeneration phase occurs when the clock signal is high (*id.* ¶ 9). The Inventors disclose that in clock transitions from high to low when the input signal is greater than the reference signal, transitional dips in signals to a latch stage can affect output performance, particularly if these dips swing far enough to cause a change in the latch output (*id.* ¶ 12). In addition, a mismatch or offset between input transistors on each side may cause the wrong intended one of these transistors to enable, thereby providing an erroneous input to the latch state (*id.* ¶ 14). The Inventors disclose that prior attempts to address these problems have required greater power consumption (*id.* ¶ 16). Therefore, the Inventors disclose the

[7] Appellant's admitted prior art, Figure 1, filed November 25, 2015 ("AAPA").

invention attempts to address these problems while reducing power consumption (*id.* ¶ 43).

Claim 1, reproduced below from the Claims Appendix to the Appeal Brief, is illustrative of the subject matter on appeal.

1. A comparator circuit, comprising:
    a first output node operable to receive a voltage during a precharge phase;
    a second output node operable to receive the voltage during the precharge phase;
    a first selectable current path, comprising a first transistor coupled between a first supply voltage terminal and the first output node, a second transistor, a first resistor coupled between the first output node and the second transistor, and a first clock transistor connected in series with a first input transistor between the second transistor and a second supply voltage terminal for selectively discharging the first output node; and
    a second selectable current path, comprising a third transistor coupled between the first supply voltage terminal and the second output node, a fourth transistor, a second resistor coupled between the second output node and the fourth transistor, and a second clock transistor connected in series with a second input transistor between the fourth transistor and the second supply voltage terminal for selectively discharging the second output node in complementary operation with respect to the first selectable current path.

Remaining independent claims 18 and 24 recite similar comparator circuits.

ANALYSIS

Appellant does not argue the claims or the rejections separately. We select claim 1 to address Appellant's argument—the remaining claims 2–10 and 18–27 stand or fall with claim 1.

The Examiner finds Eimitsu discloses a comparator circuit having a half-latch comprising transistors P1a, P1b and resistors R1a and R1b, but fails to disclose a full-latch (Final Act. 2). However, the Examiner finds Inoue discloses a similar differential circuit comprising transistors M4, M6 coupled to transistors M3, M5 and resistors R1, R2 to form a full latch. The Examiner concludes that it would have been obvious to add transistors to Eimitsu's circuit as taught in Inoue "for the purpose of forming a full-latch and providing more precise output signals" (*id.*).[8]

The Examiner acknowledges that the modified circuit fails to show a pre-charge circuit, but finds Ho teaches a differential circuit having pre-charge elements including transistors 110, 210, 118, 218 coupled between a full latch and differential input transistors, and between the power supply voltage and its outputs (Final Act. 2–3). The Examiner concludes that it would have been obvious to further add pre-charge transistor elements to Eimitsu's circuit between the full-latch and differential input transistors N1a, N1b, and between supply voltage and output nodes OUTa, OUTb, as taught in Ho, "for the purpose of using the modified circuit as a flip flop with stable duty" (*id.* at 3).

Appellant repeats the Examiner's obviousness statements (Appeal Br. 6) and sets forth a statement of the law on obviousness (*id.* at 6–11). Appellant then states that it appears that the Examiner's rejection is based solely on hindsight and, again, repeats the Examiner's obviousness statements (*id.* at 11). Thereafter, Appellant contends that the Examiner has relied on hindsight reconstruction to pick and choose among isolated

[8] Because the Examiner relies on Kalb for a feature, variable resistors, not found in claim 1, we need not discuss this reference herein.

disclosures in the prior art, implying that the rejections are based on merely conclusory statements (*id.*).

We review the appealed rejections for error based upon the issues identified by Appellant and in light of the arguments and evidence produced thereon. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) ("Filing a Board appeal does not, unto itself, entitle an appellant to *de novo* review of all aspects of a rejection. If an appellant fails to present arguments on a particular issue — or, more broadly, on a particular rejection — the Board will not, as a general matter, unilaterally review those uncontested aspects of the rejection."), *cited with approval in In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011) ("[I]t has long been the Board's practice to require an applicant to identify the alleged error in the examiner's rejections.")).

Appellant's argument is not persuasive of reversible error. "Any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning, but so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made and does not include knowledge gleaned only from applicant's disclosure, such a reconstruction is proper." *In re McLaughlin*, 433 F.2d 1392, 1395 (CCPA 1971).

We find that the Examiner supported each of the obviousness statements with both extensive specific fact finding and articulated reasoning. Appellant's argument repeatedly restates the Examiner's obviousness statements and simply contends that the Examiner has engaged in impermissible hindsight. However, Appellant does not present any argument to explain why the Examiner's explicit fact finding and articulated reasoning is not supported by the teachings of the applied prior art. Where,

as here, the Examiner has articulated reasoning with specific rational underpinning for making the proposed combination of prior art teachings, Appellant bears the burden of explaining why this reasoning is ineffective to support the conclusion of obviousness. *Cf. In re Baxter Travenol Labs.*, 952 F.2d 388, 391 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art."). Because Appellant fails to carry this burden, we sustain the Examiner's obviousness rejection of claim 1 as well as that of claims 2–10 and 18–27.

DECISION

Upon consideration of the record, and for the reasons given above and in the Final Office Action and the Examiner's Answer, the decision of the Examiner rejecting claims 1–10 and 18–27 as unpatentable under 35 U.S.C. § 103 is *affirmed.*

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

AFFIRMED