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CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
PHAM, THANHHA S

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte KUO TUNG CHANG,
CHUN CHEN, and SHENQING FANG

Appeal 2018-001342
Application 15/088,855
Technology Center 2800

Before LINDA M. GAUDETTE, MONTÉ T. SQUIRE, and MERRELL C. CASHION, JR., *Administrative Patent Judges*.

CASHION, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's decision to reject claims 1–6. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

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[1] Cypress Semiconductor Corporation is the Applicant/Appellant and is also identified as the real party in interest. Appeal Br. 1.

The subject matter of the invention is generally directed to embedded semiconductor products comprising non-volatile memory cells integrated with one or more types of non-memory transistors on the same substrate. Spec. ¶ 2, 6. Claim 1 illustrates the subject matter on appeal and is reproduced below (formatting added):

1. A semiconductor device, comprising:

a substrate comprising a core region and a peripheral region, wherein the core region is adjacent to the peripheral region;

a memory array comprising non-volatile memory cells, wherein the non-volatile memory cells are located in the core region of the substrate;

a high-voltage control logic comprising high-voltage transistors, wherein the high-voltage transistors are located in the peripheral region of the substrate; and

a low-voltage control logic comprising low-voltage transistors, wherein the low-voltage transistors are located in the peripheral region of the substrate.

Appellant (*see generally* Appeal Brief) requests review of the following rejections from the Examiner's Final Office Action:[2]

I. Claims 1–4 and 6 rejected under pre-AIA 35 U.S.C. § 102(b) as anticipated by Tanaka (US 2005/0258474 A1, published November 24, 2005).

II. Claims 1 and 3–6 rejected under pre-AIA 35 U.S.C. § 102(b) as anticipated by Smayling (US 5,844,839, issued December 1, 1998).

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[2] The Examiner withdrew the alternative rejections under 35 U.S.C. § 103(a) respectively based on Tanaka and Smayling. Ans. 2. Accordingly, we limit our discussion to the noted anticipation rejections.

In addressing both rejections, Appellant presents arguments only for independent claim 1. *See generally* Appeal Br. Accordingly, we select claim 1 as representative of the subject matter before us for review on appeal and decide the appeal as to all grounds of rejection based on the arguments made by Appellant in support of patentability of claim 1.

OPINION

The Prior Art Rejections

After review of the respective positions provided by Appellant in the Appeal and Reply Briefs[3] and the Examiner in the Final Action and Answer, we affirm the Examiner's prior art rejections of claims 1–6 under 35 U.S.C. § 102(b) for the reasons presented by the Examiner. We add the following for emphasis. We address both anticipation rejections together.

We refer to the Examiner's Final Action for statements of the rejections. Final Act. 2–4. Briefly, the Examiner finds that Tanaka's

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[3] We have considered the arguments in the Reply Brief filed November 20, 2017 in our deliberation to the extent that they are consistent with the Appeal Brief. We note, however, that Appellants present a number of arguments for the first time, such as an argument that the cells relied upon by the Examiner as memory cells are not memory cells (*see* Reply Br. 3–4). Any argument not presented in the Appeal Brief will not be considered when filed in a Reply Brief, absent a showing of good cause explaining why the argument could not have been presented in the Appeal Brief. *See Ex parte Borden*, 93 USPQ2d 1473, 1474 (BPAI 2010) (informative) ("The [R]eply [B]rief is not an opportunity to make arguments that could have been made during prosecution, but were not. Nor is the [R]eply [B]rief an opportunity to make arguments that could have been made in the principal brief on appeal to rebut the Examiner's rejections, but were not."); *see also* 37 C.F.R. § 41.41(b)(2). Appellants have not shown good cause why these arguments should now be considered.

embodiment illustrated in Figure 57 and Smayling's embodiment illustrated in Figure 3k both anticipate the subject matter of claim 1. *Id.*

Appellant argues that Tanaka and Smayling do not use Appellant's nomenclature to describe the components of the claimed semiconductor. App. Br. 4–6, 8–9. Patentability of the structure cannot turn on the use or function of the structure. *In re Michlin*, 256 F.2d 317, 320 (CCPA 1958) ("It is well settled that patentability of apparatus claims must depend upon structural limitations and not upon statements of function."). The Examiner provided an annotated copy of Tanaka's Figure 57 illustrating how the components of this structural embodiment correspond with the components of the claimed structure for Appellant's convenience. Ans. 3. Similarly, the Examiner explains in the Final Action how the elements in the structure of Smayling's embodiment correspond with each component of the claimed semiconductor device. Final Act. 4; *see also* Ans. 6–7. As the Examiner notes, using the terms "core region" and "peripheral region" to describe elements of the claimed invention does not distinguish the claimed structure from the structure disclosed by either Tanaka or Smayling. *Id.* at 4. Appellant's arguments do not point to any structural differences nor do they adequately explain why the descriptive terms used in the claims define structural differences.

Appellant argues that Tanaka does not disclose two memory cells. App. Br. 6. According to Appellant, the cells SG1 and SG2 designated by the Examiner as memory cells are instead selection (not memory) MOS transistors. *Id.* (citing Tanaka ¶ 184).

Appellant's arguments are unpersuasive. We note that Tanaka, like Appellant, discloses a memory cell/region to include a select gate (SG) and a

memory gate (MG). *Compare* Tanaka's Figure 42, *with* Appellant's Figure 3. Further, Tanaka's paragraph 184, in addition to identifying the selection gates, also discloses that the formation of the selection gates is tied with the formation of a drain region for the memory MOS transistor. Thus, as the Examiner explains (Ans. 4–6), Tanaka's disclosure points to a memory cell. While Appellant argues that Figure 57 does not show or describe a memory array (App. Br. 5), we note that Tanaka is directed to a semiconductor device including a plurality of nonvolatile memory cells. Tanaka ¶¶ 11, 31. Therefore, Appellant has not adequately explained why the components designated by the Examiner are not memory cells.

Accordingly, we affirm the Examiner's anticipation rejections of claims 1–6 for the reasons presented by the Examiner and given above.

ORDER

The Examiner's prior art rejections of claims 1–6 under 35 U.S.C. § 102(b) are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED