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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/317,691	06/27/2014	Christopher H. Olson	6000-67600	1377

58467 7590 10/29/2018

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EXAMINER	
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ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
10/29/2018	ELECTRONIC

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte CHRISTOPHER H. OLSON, JEFFREY S. BROOKS, and ALBERT DANYSH

Appeal 2018-000544
Application 14/317,691
Technology Center 2100

Before JOSEPH L. DIXON, JAMES R. HUGHES, and DENISE M. POTHIER, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants[1,2] appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1–20. *See* Appeal Br. 9. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

Invention

Appellants' invention relates to an apparatus, method, and system "disclosed for performing arithmetic operations." Spec., Abstract.

Claim 1 is reproduced below:

> 1. An apparatus, comprising:
> a fetch unit configured to retrieve a first operand and a second operand responsive to receiving an instruction, wherein a value of the first operand and a value of the second operand each include respective binary-coded decimal (BCD) values;
> an arithmetic logic unit (ALU) configured to:
> scale the value of the first operand and the value of the second operand to generate a first scaled value and a second scaled value, respectively;
> compress the first scaled value to generate a first compressed value;
> compress the second scaled value to generate a second compressed value by replacing a fractional portion of the second scaled value with a non-BCD value;
> wherein a number of data bits included in the first compressed value is less than a number of data bits included in the first scaled value, and a number of data bits included in the second compressed value is less than a number of data bits included in the second scaled value; and

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[1] Throughout this opinion, we refer to (1) the Non-Final Action (Non-Final Act.) mailed December 30, 2016, (2) the Appeal Brief (Appeal Br.) filed June 28, 2017, (3) the Examiner's Answer (Ans.) mailed August 23, 2017, and (4) the Reply Brief (Reply Br.) filed October 20, 2017.

[2] The real party in interest is listed as Oracle International Corporation. Appeal Br. 3.

> estimate a portion of a result of an operation associated with the instruction dependent upon the first compressed value and the second compressed value.

Appeal Br. 28 (Claims App.).

The Rejection

Claims 1–20 are rejected under 35 U.S.C. § 101 as being directed to patent-ineligible subject matter. Non-Final Act. 2–3.

THE CONTENTIONS

Claims 1, 5, 7, 8, 12, 14, 15, 19, and 20

Appellants argue claims 1, 5, 7, 8, 12, 14, 15, 19, and 20 as a group. Appeal Br. 14. We select claim 1 as representative. *See* 37 C.F.R. § 41.37(c)(1)(iv).

The Examiner determines claim 1 is directed to "[m]athematical algorithms and manipulation of numbers" similar to *Gottschalk v. Benson*, 409 U.S. 63 (1972) (Non-Final Act. 2) and "performing division, which is defined by mathematical relationships" (Ans. 2). The Examiner identifies the additional elements in the claims to include a processor, memory, an interface, an execution unit, a fetch unit, an ALU, a load store unit, and a data cache. Non-Final Act. 3; Ans. 3. The Examiner describes the processor, memory, and interface as general purpose computers and the other elements as being claimed at "a high level of generality" (Non-Final Act. 3) that are not "a particular machine" (Ans. 2). The Examiner states these elements perform the basic functions of the mathematical algorithms, number manipulation, and operand/instruction retrieval and storage, which

are not significantly more than the noted abstract idea. Non-Final Act. 2–3; Ans. 3.

Appellants argue the Examiner overgeneralizes claim 1 and that claim 1 is purportedly drawn to chip architecture "defin[ing] the logical organization of a 'chip' (i.e., an integrated circuit) into different circuits having different operational roles." Appeal Br. 15; *see* Appeal Br. 16 (reproducing the Specification's Figure 3) and Reply Br. 2–3. Appellants assert claim 1 is drawn to an appropriately claimed portion of chip architecture that is not abstract similar to *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1335 (Fed. Cir. 2016). Appeal Br. 17, 19. Appellants further contend the claimed compressing and estimating properties are specific improvements in an integrated circuit's or computer's operation (Appeal Br. 17–18), including "speed, size, and power benefits." Appeal Br. 17 (citing Spec. ¶¶ 72, 75), 19, 23. Appellants also argue the claimed "fetch unit" and "arithmetic logic unit" are not general purpose computers but are "specialized physical component[s]," unlike the claims in *Benson*. Appeal Br. 18 (bolding and italics omitted). Appellants argue the ALU's operation is a specialized hardware circuitry designed to compress scaled values and to estimate a result based on the compressed values, and when taking these features as an ordered combination, the design involves an inventive concept that is significantly more than any abstract idea. Appeal Br. 22–23.

ISSUE

Under § 101, has the Examiner erred in concluding claim 1 is directed to patent-ineligible subject matter?

ANALYSIS

Based on the record before us, we are not persuaded of error. In *Mayo Collaborative Services v. Prometheus Laboratories, Inc.*, 566 U.S. 66, 70 (2012) and *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 134 S. Ct. 2347 (2014), the Court set forth a two-step analytical framework for evaluating patent-eligible subject matter. First, "determine whether the claims at issue are directed to a patent-ineligible concept," such as an abstract idea. *Alice*, 134 S. Ct. at 2355. If so, "consider the elements of each claim both individually and 'as an ordered combination' to determine whether the additional elements" add enough to transform the "nature of the claim" into "significantly more" than a patent-ineligible concept. *Id.* at 2355, 2357 (quoting *Mayo*, 566 U.S. at 79).

Mayo/Alice Step 1

Step one in the *Mayo/Alice* framework involves looking at the "focus" of the claims at issue and their "character as a whole." *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016); *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1335 (Fed. Cir. 2016). This "inquiry applies a stage-one filter to claims, considered in light of the specification, based on whether 'their character as a whole is directed to excluded subject matter.'" *Enfish*, 822 F.3d at 1335 (quoting *Internet Patents Corp. v. Active Network, Inc.*, 790 F.3d 1343, 1346 (Fed. Cir. 2015)).

We agree with the Examiner that claim 1's focus is directed to mathematical algorithms and manipulation of numbers. Non-Final Act. 2. Like *Benson*, the heart of claim 1 is a sequence of instructions or functions for a digital computer (e.g., a fetch unit or ALU). *See Benson*, 409 U.S. at 65. To be sure, claim 1 recites "a fetch unit" and an "ALU" configured to

perform operations. Appeal Br. 28 (Claims App.). But, claim 1, as a whole, *focuses* on retrieving and scaling operand values (e.g., a mathematical algorithm or manipulating numbers), generating scaled values through compression so that the number of data bits in a first and second compressed value is less the number of data bits in the first and second scaled value (e.g., manipulating numbers), and estimating a portion of a result dependent on the compressed values (e.g., an algorithm or manipulating numbers). *See* Non-Final Act. 2 (citing *Benson*). We thus are not persuaded the Examiner overgeneralizes claim 1. *See* Appeal Br. 15.

The Specification also supports the claimed functions are drawn to mathematical algorithms that compute or manipulate numbers as part of a division operation. Spec. ¶¶ 67, 71, 80, Figs. 6–7, steps 605, 702 (describing scaling operand values by shifting the decimal place of an operand), ¶¶ 72–74, 80, Figs. 6–7, steps 606, 703 (describing compressing a number by truncating a value to an integer value or compressing a fractional part into a fixed number of bits that is less than original number of bits, such as from 0.63333 to two or three binary bits (e.g., "10" or "101")), ¶¶ 75, 81–83, Figs. 6–7, steps 607, 704-709 (computing minimum and maximum values to determine if values provides enough accuracy for most calculations). Court cases further demonstrate claim 1's steps of gathering, computing, and manipulating information (e.g., operands, operand values, compressed values, scaled values, and a result portion) are directed to an abstract idea. *See Elec. Power Grp.*, 830 F.3d at 1353 and *Content Extraction & Transmission LLC v. Wells Fargo Bank, Nat'l Ass'n*, 776 F.3d 1343, 1347 (Fed. Cir. 2014).

We are not persuaded that claim 1 is drawn to non-abstract, chip architecture. Appeal Br. 15–17, 19. Granted, *Enfish* indicates "some improvements in computer-related technology when appropriately claimed are undoubtedly not abstract, such as a chip architecture." *Enfish*, 822 F.3d at 1335, *cited in* Appeal Br. 12. However, *Enfish* does not elaborate on what chip architecture is *appropriately claimed* so that its architecture is not abstract. *See id.* Additionally, we disagree that claim 1's focus is drawn to chip architecture that defines its logical organization. *See* Appeal Br. 9, 15–17. Rather, claim 1 recites two components of "an apparatus"—"a fetch unit" and an "ALU"—and does not recite sufficiently how these components interact, are connected, or are implemented as Appellants discussed. *See* Reply Br. 3 (discussing Figure 3 and implementing Figure 3's elements using static logic, dynamic logic, field effect transistors, or bipolar junction transistors). Rather, as previously discussed, claim 1 recites how the units are configured to perform steps of gathering, computing, and manipulating values directed to abstract ideas. *See* Appeal Br. 28 (Claims App.). Appellants' arguments are therefore not commensurate in scope with claim 1.

Appellants further contend the claimed features of an ALU configured to "compress" scaled values and "estimate" a portion of an operation's result dependent on the compressed values recite specific improvements in an integrated circuit's or computer's operation. Appeal Br. 17–18. Namely, Appellants identify "speed, size, and power benefits." Appeal Br. 17 (citing Spec. ¶¶ 72, 75); *see also* Appeal Br. 9–10, 19, and 23. Appellants also argue the claimed "fetch unit" and "arithmetic logic unit" are not general purpose computers but are "specialized physical component[s]," unlike the

claims in *Benson*. Appeal Br. 18 (bolding and italics omitted); *see also* Appeal Br. 13–14. These arguments are unavailing.

First, we recognize the Specification states compressing a number reduces the number of bits (Spec. ¶ 72) and estimating the next digit "may be simpler, allowing for faster processing time and/or smaller, more power efficient circuitry in ALU 340" (Spec. ¶ 75). However, we stress the disclosure indicates the calculations *may* be simpler and thus, the alleged improvement of a faster, smaller, and power-efficient apparatus (Appeal Br. 17) is not necessary achieved through the broadly recited compression and estimation in claim 1. Moreover, several court decisions indicate "merely adding computer functionality to increase the speed or efficiency of the process does not confer patent eligibility on an otherwise abstract idea." *Intellectual Ventures I LLC v. Capital One Bank (USA)*, 792 F.3d 1363, 1370 (Fed. Cir. 2015); *see also Credit Acceptance Corp. v. Westlake Services*, 859 F.3d 1044, 1057 (Fed. Cir. 1057) (quoting *Capital One Bank*, 792 F.3d at 1370).

Second, claim 1 differs from the claims in *Enfish*. For example, claim 1 does not recite a specific data structure designed to improve the way a computer stores and retrieves data from memory (i.e., a self-referential table). *See Enfish*, 822 F.3d at 1335-39; *see also* Ans. 4. Rather, as noted above, claim 1 is directed to apparatus having components (i.e., a fetch unit and an ALU) configured to collect, compute, and manipulate values. Appeal Br. 28 (Claims App.).

Third, in contrast with Appellants' contentions (Appeal Br. 13), *Benson* does identify an entity (i.e., a shift register) responsible for performing various steps. *See* Appeal Br. 12–13. Additionally, regardless

of whether an ALU is a complete processor (Appeal Br. 18), we disagree that claim 1's focus is drawn to specialized physical component or a specialized circuity (Appeal Br. 18–19) for reasons previously stated. Rather, claim 1 is directed to a generalized formulation to solve arithmetic operations. Appeal Br. 28 (Claims App.); *see also* Spec. ¶ 1. Furthermore, courts have treated "analyzing information by steps people go through in their minds, or by mathematical algorithms, without more, as essentially mental processes within the abstract-idea category."' *Elec. Power Grp.*, 830 F.3d at 1354. We further note that "[t]hat purely mental processes can be unpatentable, even when performed by a computer, was precisely the holding of the Supreme Court in *Gottschalk v. Benson*." *CyberSource Corp. v. Retail Decisions, Inc.*, 654 F.3d 1366, 1375 (Fed. Cir. 2011).

Notably, independent claim 8 recites a method claim and not an apparatus, similarly focusing on mathematical algorithms or manipulation of numbers. Appeal Br. 29–30 (Claims App.). This claim further recites steps of storing operands (Appeal Br. 29 (Claims App.); *see* Non-Final Act. 2), which is similarly drawn to an abstract idea. *See In re TLI Comm'ns LLC Patent Litigation*, 823 F.3d 607, 611 (Fed. Cir. 2016).

Independent claim 15 recites a system claim similarly focused on the mathematical algorithms and number manipulation. Appeal Br. 31–32 (Claims App.). Granted, claim 15 recites "an interface configured to couple the processor and the memory," but such a broad recitation does not amount to the appropriately claimed, chip architecture that is not abstract identified in *Enfish*. Like claim 8, claim 15 recites "a memory configured to store one or more program instructions" (Appeal Br. 31 (Claims App.)), but that recitation is drawn to an abstract idea.

Accordingly, when considering claim 1's character as a whole (as well as claims 8 and 15) consistent with the Specification, the claim's focus is directed to at least one abstract idea.

Mayo/Alice Step 2

Because we determine claim 1 is directed to at least one abstract idea, we proceed to analyze the claim under step two. We consider the elements of claim 1 both individually and as a combination to determine whether the additional elements add enough to transform the claim's nature into significantly more than a patent-ineligible concept. Step two involves the search for an "inventive concept." *Alice*, 134 S. Ct. at 2355; *Elec. Power Grp.*, 830 F.3d at 1353. An "inventive concept" requires more than "well-understood, routine, conventional activity already engaged in" by the relevant community. *Rapid Litig. Mgmt. Ltd. v. CellzDirect, Inc.*, 827 F.3d 1042, 1047 (Fed. Cir. 2016) (quoting *Mayo*, 566 U.S. at 79–80).

The Examiner identifies the additional elements in the claim 1 as a fetch unit and an ALU. Non-Final Act. 3. The Examiner states these elements perform basic functions of implementing mathematical algorithms, number manipulation, and operand/instruction retrieval, which do not amount to significantly more than the abstract idea. Non-Final Act. 2–3. We agree. For example, an ALU is described in the Specification as a unit that performs arithmetic operations, Boolean operations, and other desired functions, including formatting numbers. Spec. ¶¶ 3–4. Also, the Specification describes a fetch unit as a unit that prepares instruction for execution. Spec. ¶ 3. Thus, the claimed functions performed in claim 1 (e.g., scale, compress, and estimate information and retrieve operands responsive to an instruction) include those an ALU and a fetch unit routinely

and conventional do. We therefore disagree claim 1's additional elements are non-conventional and non-generic as asserted. Appeal Br. 23.

Moreover, we disagree that claim 1, including the ALU and the fetch unit, recites a specialized circuit that improves on a computer's functioning or technology (*see* Appeal Br. 22–23, and 25; Reply Br. 4–5), such that claim 1's additional elements add enough to transform the claim into significantly more than a patent-ineligible concept. Rather, the ALU and fetch unit are merely tools used to perform the claim's functions. *See Alice*, 134 S. Ct. at 2358 (holding "the mere recitation of a generic computer cannot transform a patent-ineligible abstract idea into a patent-eligible invention"). Also, as previously stated, "merely adding computer functionality to increase the speed or efficiency of the process does not confer patent eligibility on an otherwise abstract idea." *Capital One Bank*, 792 F.3d at 1370. To the extent claim 1 does recite chip architecture, "limiting the claims to a particular technological environment . . . is, without more, insufficient to transform them into patent-eligible applications of the abstract idea at their core." *Elec. Power Grp.*, 830 F.3d at 1354; *see also Alice*, 134 S.Ct. at 2358.

Independent claims 8 and 15 further recite other additional elements, including a processor, memory, an interface, an execution unit, a load store unit, and a data cache. Non-Final Act. 3; Ans. 3. The Examiner describes the processor, memory, and interface as general purpose computers and the other elements as being claimed at "a high level of generality." Non-Final Act. 3. We agree. These elements are similarly computer tools that do no more than implement the above-discussed abstract ideas (e.g., compute mathematical algorithms and manipulate numbers) and do not add enough to

transform the claim's nature into significantly more than an abstract idea. *See* Non-Final Act. 2–3; Ans. 3.

Appellants lastly argue claim 1 does not preempt all the uses of the alleged mathematical algorithm or any abstract idea because the claims are directed to a particular chip architecture. *See* Appeal Br. 24–25. We are not persuaded. Lack of preemption does not make a claim any less abstract. *See Ariosa Diagnostics, Inc. v. Sequenom, Inc.*, 788 F.3d 1371, 1379 (Fed. Cir. 2015) ("While preemption may signal patent ineligible subject matter, the absence of complete preemption does not demonstrate patent eligibility"); *see also See Parker v. Flook*, 437 U.S. 584, 589 (1978) and Ans. 4.

For the above reasons, claim 1's limitations, viewed both individually and as an ordered combination, do not amount to significantly more than a judicial exception and do not sufficiently transform the nature of the claim into patent-eligible subject matter. Accordingly, Appellants have not persuaded us the Examiner erred in the rejecting independent claim 1 and claims 5, 7, 8, 12, 14, 15, 19, and 20, which are not separately argued.

Claims 2–4, 6, 9–11, 13, and 16–18

Appellants argue dependent claims 2, 9, and 16 as a group. Appeal Br. 19–20, 25–26. Claims 3, 4, 6, 10, 11, 13, 17, and 18 depend directly or indirectly from one of claims 2, 9, and 16 and are not separately argued. We select 2 as representative. *See* 37 C.F.R. § 41.37(c)(1)(iv).

Appellants assert claim 2 adds a "lookup table" feature. Appeal Br. 19. According to Appellants, the lookup table may be more compact and may be significantly faster to access, adding a specific improvement in computer performance. Appeal Br. 19–20 (citing Spec. ¶¶ 85, 91). For this reason and because the lookup table enables a more compact circuit design,

Appellants contend claim 2 recites significantly more than an abstract idea. Appeal Br. 25–26.

Claim 2 recites a more detailed version of how the ALU is configured to "estimate a portion of a result of an operation," which is part of the above-identified abstract idea. Given the record, we agree claim 2 is directed to an abstract idea. Non-Final Act. 2; Ans. 2. Also, the Specification states the "[*i*]*f the lookup table is small enough*, using the lookup table *may provide* a speed improvement versus calculating Qmax and Qmin for each digit of the quotient." Spec. ¶ 85 (italics added). Accordingly, the lookup table must be *small enough* and even then, the table *may provide* a speed improvement. Spec. ¶ 85. Claim 2 does not recite the size of the lookup table, such that the alleged improved feature is claimed. Similarly, cited paragraph 91 states the lookup table "*may provide* a more efficient method for determining Qmin and Qmax," but does not necessary provide the noted efficiency. Spec. ¶ 91 (italics added). Even more, as previously stated, "merely adding computer functionality to increase the speed or efficiency of the process does not confer patent eligibility on an otherwise abstract idea." *Capital One Bank*, 792 F.3d at 1370. Thus, the recited "lookup table" that *may* increase speed or efficiency does not add enough to transform claim 2's nature into significantly more than a patent-ineligible concept.

Appellants further contend the lookup table "*may enable* more compact circuit design" than "circuitry for directly calculating a result." Appeal Br. 26 (italics added). The Specification at best describes the size of the "lookup table"— not the circuitry's size—*may impact* the speed of the system. *See* Spec. ¶ 85. Moreover, this explanation suffers from the same some problem as noted in the previous paragraph. That is, the broadly

claimed "lookup table" does not specify a speed improvement or a more compact circuit design. As such, Appellants' arguments are not commensurate in scope with claim 2.

When considering the elements of claim 2 both individually and as a combination, we determine claim 2's additional elements do not add enough to transform the claim into significantly more than a patent-ineligible concept. Accordingly, Appellants have not persuaded us the Examiner erred in the rejecting claim 2 and claims 3, 4, 6, 9–11, 13, and 16–18, which are not separately argued.

DECISION

We affirm the Examiner's rejection of claims 1–20 under 35 U.S.C. § 101.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED