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NIXON & VANDERHYE, P.C.
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER
PAN, DANIEL H

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ALASTAIR DAVID REID and DANIEL KERSHAW

Appeal 2017-011426
Application 14/461,664[1]
Technology Center 2100

Before JUSTIN BUSCH, CATHERINE SHIANG, and
CARL L. SILVERMAN, *Administrative Patent Judges*.

SILVERMAN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection[2] of claims 1–6, 10–12, 14–17, 20–22, and 25–28. Claims 1–28 are pending. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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[1] The real party in interest is identified as ARM Limited. App. Br. 3.

[2] The Examiner finds "Claim 7–9, 13, 18, 19, 23, 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." Final Act. 18.

STATEMENT OF THE CASE

The claimed invention relates to controlling performance of speculative vector operations, particularly providing "a mechanism for performing speculative vector operations whilst managing the impact of such speculative vector processing on a performance characteristic of the apparatus." Abstract; Spec. 2:29–4:5, Fig. 1. Claim 1, reproduced below, is exemplary of the subject matter on appeal (emphasis added):

> 1. A data processing apparatus comprising:
>
> *processing circuitry configured to perform a sequence of speculative vector operations on vector operands*, each vector operand comprising a plurality of vector elements;
>
> speculation control circuitry configured to maintain *a speculation width indication indicating the number of vector elements of each vector operand to be subjected to said speculative vector operations*, the speculation width indication *being initialised to an initial value prior to performance of said sequence of speculative vector operations*;
>
> said processing circuitry *being configured to generate progress indications during performance* of said sequence of speculative vector operations;
>
> *the speculation control circuitry being further configured to detect, with reference to the progress indications and speculation reduction criteria, presence of a speculation reduction condition, the speculation reduction condition being a condition indicating that a reduction in the speculation width indication is expected to improve at least one performance characteristic of the data processing apparatus relative to continued operation without the reduction in the speculation width indication*;
>
> the speculation control circuitry being further responsive to detection of said speculation reduction condition *to reduce the speculation width indication*.

App. Br. 17.

THE REJECTIONS

Claim 27 is rejected under 35 U.S.C. § 112(b) as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventors regard as the invention. Final Act. 2.

Claims 1–6, 12, 14–17, 20–22, 25, 26, and 28 are rejected under 35 U.S.C. § 102(a)(1) as being anticipated by Gonion et al. (US 2008/0288744 A1; pub Nov. 20, 2008) ("Gonion"). Final Act. 3–11.

Claims 10 and 11 are rejected under 35 U.S.C. § 103 as being unpatentable over Gonion in view of Singh (US 6,915,395 B1; iss. July 5, 2005) ("Singh"). Final Act. 12–13.

Claim 27 is rejected under 35 U.S.C. § 103 as being unpatentable over Gonion in view of Nakajima et al. (US 5,511,217; iss. Apr. 23, 1996) ("Nakajima"). Final Act. 13–14.

ANALYSIS

The § 112 Rejection

The Examiner finds it is unclear whether claim 27 (non-transitory computer readable storage medium storing instructions), which depends from claim 1 (data processing apparatus), is directed to a non-transitory computer-readable storage medium (also referred to as "CRM") or a data processing apparatus. Final Act. 2. In the Answer, the Examiner finds "the physical relation between the storage medium and the data processing apparatus is unclear." Ans. 20–21. The Examiner finds the specification teaches a host processor and a data processing system but neither the specification nor the claim teaches the structural connection between the host processor and the data processing apparatus, and, "[t]herefore, it

is unclear whether the CRM in claim 27 is part of the data processing apparatus or separate from the data processing apparatus? And, for this reason, the meaning of the claim scope is unclear." *Id.*

Appellants argue claim 27 is a CRM claim "that stores a computer program that controls a computer *to provide a virtual machine execution environment* for program instructions *that corresponds to* a data processing apparatus as claimed in Claim 1." App. Br. 15. In the Reply Brief, Appellants argue claim 27 is a CRM claim and it can be part of, or separate from, the data processing apparatus. Reply Br. 8. According to Appellants, "[a]ll that is required is the CRM store a computer program that can be used to control a computer to 'provide a virtual machine execution environment for program instructions corresponding to a data processing apparatus as claimed in Claim 1.'" Appellants argue "[t]here is no need to specify whether the CRM 'is part of the data processing apparatus or separate from the data processing apparatus' in order for a POSA to understand what is being claimed in claim 27." *Id.*

We are persuaded by Appellants' arguments regarding indefiniteness based on the understanding of one of ordinary skill in the art. *In re Packard*, 751 F.3d 1307 (Fed. Cir. 2014). As Appellants emphasized, claim 27 recites a CRM with a viritual machine execution environment program, where the virtual machine execution environment corresponds to the data processing apparatus recited in claim 1. In other words, the recited CRM stores a program that provides a virtual machine having virtual hardware that emulates the data processing apparatus recited in claim 1.

In view of the above, we do not sustain the rejection of claim 27.

The § 102 Rejections

Appellants argue, *inter alia*, the Examiner errs in finding Gonion discloses the claim 1 limitation:

> *the speculation control circuitry being further configured to detect, with reference to the progress indications and speculation reduction criteria, presence of a speculation reduction condition, the speculation reduction condition being a condition indicating that a reduction in the speculation width indication is expected to improve at least one performance characteristic of the data processing apparatus relative to continued operation without the reduction in the speculation width indication.*

("disputed limitation") App. Br. 7–14; Reply Br. 2–7.

Appellants describe high performance implementations which utilize vector processing circuitry which performs the required operation in parallel on the various vector elements within the vector operands. Spec. 1:19–23. Alternatively, scalar processing circuitry can be used to implement the vector operation wherein the vector operation is implemented by iterative execution of an operation by the scalar processing circuitry, with each iteration operating on different vector elements of the vector operands. *Id.* at 1:22–26. According to Appellants, the conventional vectorization approach is to process in parallel at the maximum width possible under the assumption that this leads to the greatest processing improvement, but this may lead to degradation in performance characteristics compared to using a smaller vector width. App. Br. 7–8 (citing Spec. 3:27–4:5). Appellants argue:

> although processing at the maximum vector width is still possible, (i.e., *processing is not prevented),* one or more current factors, such as the example micro-architectural events described in the application on page 5, lines 14-23, may adversely impact vector processing throughput or energy consumption relative to a smaller vector width so that processing at a smaller vector operand width (a smaller number of vector elements in the vector operand) provides better performance.

Id. at 8.

Appellants argue micro-architectural events are not architectural events because *architectural events prevent the performance of vector operations* at a specific vector width whereas *micro-architectural may negatively impact the processing performance of vector operations at a specific vector width, but they do not prevent the performance of vector operations at that vector width.* *Id.* (citing Spec. 5:24–6:3). According to Appellants, Gonion fails to recognize that occurrence of micro-architectural events can adversely impact vector processing performance and this helps to explain why Gonion does not disclose claim 1 limitations. *Id.*

Regarding the disputed limitation, the Examiner finds Gonion teaches memory hazards (read and write operations accessing the same memory location) are addressed by specifying predicate vectors that specify the elements for which memory operations may be safely performed in parallel for the given memory hazard conditions. Ans. 15–20. The Examiner finds memory hazards will cause delays and "[t]herefore, memory hazards will negatively impact the processing performance, but will not prevent the performance of vector operations at the vector width due to Gonion's predicate values (See the number of consecutive elements (vector width) that can performed safely in parallel; see para [0077])" and "[t]his teaching of Gonion is clearly a characteristic feature of a micro architectural event." *Id.* at 16.

The Examiner finds Gonion predicate vector P2 is the speculation width indicator and generates at each pass, predicate values of elements and positions. *Id.* at 16–17 (citing Gonion Figs. 3, 4). The Examiner finds P2 is

based on the stop bit P1 which covers the memory hazards and therefore "P2 is determined to include as many vector elements as possible until the next stop indicator P1, and this process is repeated in subsequent iterations for all data elements in the vector." *Id.* at 18 (citing Gonion ¶¶ 82–84). The Examiner finds Gonion's P2 is dynamically generated at each pass to indicate active elements which can achieve the greatest amount of parallelism possible for the given memory hazard conditions. *Id.* at 19 (citing Gonion ¶ 84; Fig.4).

The Examiner then finds:

> Gonion teaches clearly that P2 (the speculation width indication) indicates the elements to be processed to implement the piecewise processing of a single vector (see each pass of P2 in fig.4), and P2 can be determined iteratively, where as many vector elements are included as possible until the next stop indicator P1 (see P2 that includes 1's), and this process is repeated in subsequent iterations until all elements in the vector are included, and this technique allows to achieve the greatest amount of parallelism possible for the given hazard conditions (see Gonion [0084]). The memory hazards are indicated by the stop bit P1 (see para [0082]). Therefore, Gonion's predicate values of P2 specify elements for which the memory operations (e.g. read/write, load/store) may safely be performed in parallel for a set of consecutive elements (e.g. para [0077]).
>
> And, for the above reason, Gonion teaches that a reduction in the speculation width indication (see each pass of P2 that indicates number of active elements in fig.4) is expected to improve at least one performance characteristic (e.g. parallelism) of the data processing apparatus relative to continued operation without the reduction in the speculation width indication (i.e. without P2 or the piece wise processing the greatest possible of the amount of parallelism for the memory hazard conditions cannot be achieved; see Gonion para [0084).

Id. at 19–20.

In the Reply Brief, Appellants argue the Examiner errs in finding Gonion teaches memory hazards will cause delays but will not prevent the performance of vector width. Reply Br. 2–4 (citing Ans. 16; Gonion ¶ 6). According to Appellants, Gonion states that memory hazards can prevent parallelization of code altogether. *Id.* at 3 (citing Gonion ¶ 6, 82; Figs. 3). Appellants argue Gonion addresses memory hazards by employing check hazard iterations to create iteration control vectors P1 containing stop indicators that determine the extent to which code should be vectorized. *Id.* at 4 (citing Gonion Figs. 3, 4). According to Appellants, Gonion's first vector iteration is only the first three columns and these are performed in parallel, but a number of columns larger than three is not previously identified and, in contrast to claim 1, the number of columns is not subsequently reduced to identify a smaller subset of the first three columns. *Id.* Specifically, Appellants argue Gonion's P2 is set to identify the first three columns, is not subject to further reductions during the first pass, and vectoring beyond the first three columns is not done because, if that were done, an error in processing would occur. *Id.* Appellants further argue, rather than recognizing that it is not always best to vectorize the maximum extent possible when performing speculative vector processing, Gonion seeks to achieve the greatest amount of parallelism possible, bounded only by the stop indicators for memory hazard conditions. *Id.* at 7 (citing Gonion ¶ 84; Fig. 4).

Appellants further argue the Examiner errs in finding Gonion teaches expected improvement in "at least one performance characteristic . . . relative to continued operation without the reduction in the speculation width indication," *Id.* at 6–7. According to Appellants, although the

Answer refers to "parallelism," vectorizing code to perform parallel operations likely improves performance as compared to iterative scalar operation, but improved performance relative to an equivalent iterative sequence of scalar is not what is recited in claim 1. *Id.* (citing Ans. 19–20). Appellants argue claim 1's improved performance is in the context of one parallel operation compared to another parallel operation, not as compared to iterative scalar operation. *Id.* at 7. According to Appellants, "claim 1 identifies situations where "reduc[ing] the speculation width indication [i.e., performing a reduced level of vectorization] is expected to improve at least one performance characteristic of the data processing apparatus relative to continued operation without the reduction in the speculation width indication [i.e., maintaining a higher level of vectorization]." *Id.*

We are persuaded by Appellants' arguments that Gonion's interactive process, using P1 stop points for memory hazards, does not disclose the disputed limitation. In particular, Gonion does not disclose "the speculation reduction condition" and "reduc[ing] the speculation width indication" "responsive to detection of said speculation reduction condition." Specifically, Gonion does not disclose the recited "reduction condition" is "a condition indicating that a reduction in the speculation width is expected to improve at least one performance characteristic of the data processing apparatus *relative to continued operation without the reduction in the speculation width indication*." We note the term "performance characteristic" is described in the specification as "for example throughput or energy consumption" and is described as micro-architectural rather than architectural. Spec. 3:1–6, 3:27–4:5, 5:24–6.3. The Examiner's findings regarding Gonion disclosing the "performance characteristic" are

insufficient because Gonion's processing to avoid the memory hazards is inconsistent with the use of the term in the specification. *In re Crish*, 393 F.3d 1253, 1256 (Fed. Cir. 2004).

Therefore, the Examiner's findings do not meet the requirements for anticipation. A claim is anticipated only if each and every element as set forth in the claims is found, either expressly or inherently described in a single prior art reference, and arranged as required by the claim. *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987

In view of the above, we do not sustain the rejection of claim 1, independent claims 26 and 28 as these claims are commensurate in scope with claim 1, and dependent claims 2–6, 12, 14–17, 20–22, and 25.

Because our decision with regard to the disputed limitation is dispositive of the rejection of these claims, we do not address additional arguments raised by Appellants.

The § 103 Rejections

Dependent claims 10, 11, and 27 are rejected over the combination of Gonion with Singh or Nakajima. The additional references are not relied on to address the deficiencies of claim 1, discussed *supra*. Therefore, we do not sustain the rejection of claims 10, 11, and 27.

DECISION

We reverse the Examiner's decision rejecting claim 27 under 35 U.S.C. § 112(b).

We reverse the Examiner's decision rejecting claims 1–6, 12, 14–17, 20–22, 25, 26, and 28 under U.S.C. § 102(a)(1).

We reverse the Examiner's decision rejecting claims 10, 11, and 27 under 35 U.S.C. § 103(a).

REVERSED