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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MADHUKAR BUDAGAVI[1]

Appeal 2017-011341
Application 13/668,289
Technology Center 2100

Before JASON V. MORGAN, ERIC B. CHEN, and NABEEL U. KHAN, *Administrative Patent Judges*.

MORGAN, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Introduction

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1 and 6. Claims 2–5 and 7–10 are canceled. Ans. 2; *see also* App. Br. 2. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

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[1] Appellant is the applicant, Texas Instruments Incorporated, identified in the Appeal Brief as the real party in interest. App. Br. 2.

Invention

Appellant discloses "a unified forward and inverse transform architecture that supports computation of both forward and inverse transforms . . . using shared hardware circuits." Abstract.

Representative Claim (*key limitations emphasized*)

1. An apparatus for computation of forward and inverse transforms, the apparatus comprising:

a first decomposition circuit configured to receive an N-point input vector, wherein the first decomposition circuit is operable to decompose the N-point input vector to form a first (N/2)-point vector and a second (N/2)-point vector, wherein, in response to a control signal, the first (N/2)-point vector and the second (N/2)-point vector are inputs for an N-point forward transform computation or inputs for an N-point inverse transform computation;

a first matrix multiplication circuit coupled to the first decomposition circuit to receive the second (N/2)-point vector;

a forward and inverse (N/2)-point transform computation circuit coupled to the first decomposition circuit to receive the first (N/2)-point vector;

a first recomposition circuit coupled to receive a first (N/2)-point output vector from the first matrix multiplication circuit and a second (N/2)-point output vector from the forward and inverse (N/2)-point transform computation circuit, wherein the first recomposition circuit is operable to compose an N-point output vector from the first (N/2)-point output vector and the second (N/2)-point output vector, wherein, in response to the control signal, the N-point output vector is an output of the N-point forward transform computation or an output of the N-point inverse transform computation,

wherein the first matrix multiplication circuit is configured to multiply the second (N/2)-point vector with an (N/2) × (N/2) matrix, the (N/2) × (N/2) matrix consisting of elements from odd lines of an N×N transform coefficient matrix, and

wherein the forward and inverse (N/2)-point transform computation circuit is configured to compute an (N/2)-point forward transform or an (N/2)-point inverse transform responsive to the control signal.

Rejection

The Examiner rejects claims 1 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Fettweis (US 5,452,466; issued Sept. 19, 1995) and Pan (US 6,587,590 B1; issued July 1, 2003). Final Act. 2–10.

INVENTION SUMMARY

Claim 1 is directed to circuitry that computes one of two transforms using shared operations. These are referred to as a "forward" transform and an "inverse" transform, although there is no guarantee that the inverse transform will be the inverse of the forward transform. This lack of a guaranteed inverse relationship between the two transforms reflects the intended application of the claimed circuitry to high efficiency video coding (HEVC), which involves additional quantize and inverse quantize operations between the forward and inverse transforms. Spec. ¶¶ 3, 87, 90, and Fig. 19.

Each of the transforms is represented by the multiplication of an N×N matrix by an N-point input vector to obtain an N-point output vector. The Specification provides example forward and inverse 4-point transforms that, while non-limiting, illustrate how operations between forward and inverse transforms are shared.

The Specification discloses a forward 4-point transform of input vector $M = [M0, M1, M2, M3]^T$ to output vector $P = [P0, P1, P2, P3]^T$ using the operation $P = D_4 M$, where D_4 is given by:

$$D_4 = \begin{bmatrix} C16 & C16 & C16 & C16 \\ C8 & C24 & -C24 & -C8 \\ C16 & -C16 & -C16 & C16 \\ C24 & -C8 & C8 & -C24 \end{bmatrix}$$

Spec. ¶ 37. C8, C16, and C24 are constants defined in the 32-point HEVC core transform matrix as C8 = 83, C16 = 64, and C24 = 36. *Id.* ¶ 35.

The inverse 4-point transform of input vector $X = [X0, X1, X2, X3]^T$ to output vector $Y = [Y0, Y1, Y2, Y3]^T$ uses the operation $Y = D_4^T X$. Spec. ¶ 40.

Both the forward and inverse 4-point transforms are decomposed in slightly different ways to create matrices that, with either some pre-processing or post-processing, can be used for either transform.

The forward 4-point transform is decomposed by pre-processing input vector *M* values to produce intermediate input vector $[K0, K1, K2, K3]^T$ using addition and subtraction operations as follows:

$$\begin{bmatrix} K0 \\ K1 \\ K2 \\ K3 \end{bmatrix} = \begin{bmatrix} M0 + M3 \\ M1 + M2 \\ -M1 + M2 \\ -M0 + M3 \end{bmatrix}$$

Spec. Fig. 2.

The even output vector values are calculated from a 2×2 matrix multiplication involving two of the intermediate vector values as follows:

$$\begin{bmatrix} P0 \\ P2 \end{bmatrix} = \begin{bmatrix} \mathrm{C16} & \mathrm{C16} \\ \mathrm{C16} & -\mathrm{C16} \end{bmatrix} \begin{bmatrix} K0 \\ K1 \end{bmatrix}$$

Id.

The odd output vector values are calculated from a different 2×2 matrix multiplication involving two of the intermediate vector values as follows:

$$\begin{bmatrix} P1 \\ P3 \end{bmatrix} = \begin{bmatrix} -\mathrm{C24} & -\mathrm{C8} \\ \mathrm{C8} & -\mathrm{C24} \end{bmatrix} \begin{bmatrix} K2 \\ K3 \end{bmatrix}$$

Id.

The inverse transform is decomposed slightly differently, with the even input values used directly—using the same matrix used to produce even forward transform output vector values—to produce two values in intermediate output vector $Z = [Z0, Z1, Z2, Z3]^T$ using the following matrix multiplication:

$$\begin{bmatrix} Z0 \\ Z1 \end{bmatrix} = \begin{bmatrix} \mathrm{C16} & \mathrm{C16} \\ \mathrm{C16} & -\mathrm{C16} \end{bmatrix} \begin{bmatrix} X0 \\ X2 \end{bmatrix}$$

Id. at Fig. 3.

Similarly, the odd input values are used directly—using the same matrix used to produce odd forward transform output vector values—to produce the remaining two values in intermediate output vector *Z* using the following matrix multiplication:

$$\begin{bmatrix} Z2 \\ Z3 \end{bmatrix} = \begin{bmatrix} -\mathrm{C24} & -\mathrm{C8} \\ \mathrm{C8} & -\mathrm{C24} \end{bmatrix} \begin{bmatrix} X1 \\ X3 \end{bmatrix}$$

Id.

To produce output vector *Y* of the inverse transform, values from intermediate output vector *Z* are used in post-processing addition and subtraction operations as follows:

$$\begin{bmatrix} Y0 \\ Y1 \\ Y2 \\ Y3 \end{bmatrix} = \begin{bmatrix} Z0 - Z3 \\ Z1 - Z2 \\ Z1 + Z2 \\ Z0 + Z3 \end{bmatrix}$$

Id.

With these even-odd decompositions, referred to in the Specification as "partial butterfly decomposition[s]" (Spec. ¶ 38), a shared architecture can perform either a forward or an inverse transform. An example unified architecture for performing the 4×4 forward or inverse transforms $P = D_4 M$ and $Y = D_4^T X$ is disclosed in the Specification's Figure 7, reproduced below:

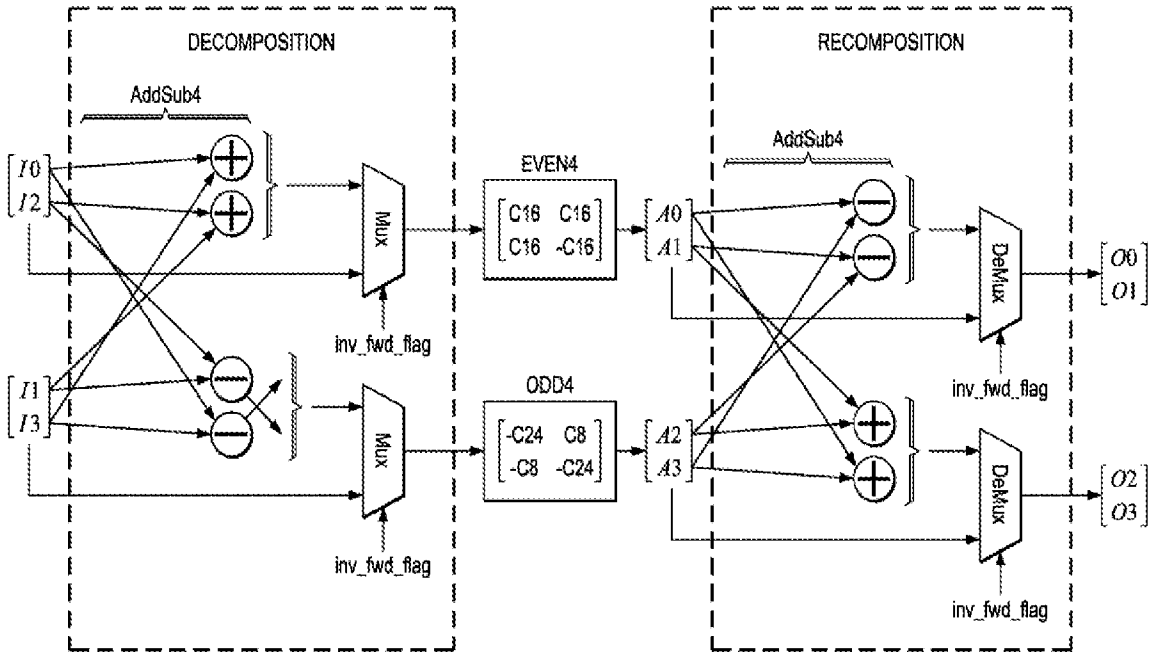

FIG. 7

The Specification's Figure 7 illustrates an architecture for performing either a forward or inverse transform using input vector $I = [I0, I1, I2, I3]^T$ (which represents M for a forward transform and X for an inverse transform), output vectors $[O0, O1]^T$ and $[O2, O3]^T$ (which represent[2] $[P0, P2]^T$ and $[P1, P3]^T$ for a forward transform or $[Y0, Y1]^T$ and $[Y2, Y3]^T$ for an inverse transform), intermediate output vectors $[A0, A2]^T$ and $[A2, A3]^T$, and a control flag (inv_fwd_flag). *See also* Spec. ¶¶ 45–46. The architecture includes decomposition components, even and odd 2×2 matrix multiplication components, and recomposition components. *Id.* at Fig. 7.

How the example architecture reads on the limitations of claim 1 is mostly straightforward. Figure 7 illustrates decomposition and

[2] The Specification's disclosure erroneously maps $O2$ to $P0$ instead of $P1$. Spec. ¶ 45. However, this mapping is inconsistent with the decomposition illustrated in the Specification's Figure 2 and the non-unified example architecture illustrated in the Specification's Figure 6.

recomposition components that read on the claimed *first decomposition circuit* and *first recomposition circuit*. And Figure 7's ODD4 matrix reads on the claimed *first matrix multiplication circuit*. The only recitations in need of additional context beyond the example 4×4 transforms architecture are the recitations directed to *a forward and inverse (N/2)-point transform computation circuit coupled to the first decomposition circuit to receive the first (N/2)-point vector, wherein the forward and inverse (N/2)-point transform computation circuit* being *configured to compute an (N/2)-point forward transform or an (N/2)-point inverse transform responsive to the control signal*.

With the 4×4 forward or inverse transform example provided in the Specification, the "forward and inverse (N/2)-point transform computation circuit" would be the even 2×2 matrix multiplication, which operates the same regardless the inv_fwd_flag value. Spec. ¶¶ 5–6. However, the Specification also discloses additional embodiments directed to architectures for at least 8×8, 16×16, and 32×32 forward or inverse transforms. *See, e.g.*, *id.* ¶¶ 47–58, Figs. 13–15. In each of these example embodiments, the even (N/2)×(N/2) matrix multiplication is identical to the forward and inverse N/2 transform disclosed in the Specification. *See id.* ¶¶ 50 ("the even matrix of the 8-pt forward transform . . . is identical to the 4-pt forward transform . . . and the even matrix of the 8-pt inverse transform . . . is identical to the 4-pt inverse transform"), and 56. Thus, these embodiments can make use of an N/2 forward or inverse transform circuit rather than a matrix multiplication to obtain the output values of the (N/2)×(N/2) even matrix multiplication. *See id.* Figs. 13–15. The recitations directed to use of a "forward and

inverse (N/2)-point transform computation circuit" appear intended to encompass these recursively-defined embodiments.

FINDINGS AND CONTENTIONS

In rejecting claim 1 under 35 U.S.C. § 103(a), the Examiner finds the discrete cosine transforms (DCT) and inverse discrete cosine transforms (IDCT) architecture of Fettweis—which includes pre-processor 3′, shuffle-exchange unit 30, and post-processor 2′—teaches or suggests most of the recitations, including *a forward and inverse (N/2)-point transform computation circuit coupled to the first decomposition circuit to receive the first (N/2)-point vector, wherein the forward and inverse (N/2)-point transform computation circuit is configured to compute an (N/2)-point forward transform or an (N/2)-point inverse transform responsive to the control signal*. Final Act. 3–4 (citing Fettweis col. 7, ll. 27–28, 32–37, 45–54, col. 8, ll. 1–5, Figs. 1, and 9–10). The Examiner relies on Pan's matrix multiplication, using an (N/2)×(N/2) matrix formed using a subset of elements from an N×N matrix, to teach or suggest *wherein the first matrix multiplication circuit is configured to multiply the second (N/2)-point vector with an (N/2) × (N/2) matrix, the (N/2) × (N/2) matrix consisting of elements from odd lines of an N×N transform coefficient matrix*. Final Act. 5 (citing Pan col. 28, ll. 37–44, col. 29, ll. 45–54, 60–64, col. 53, l. 67–col. 54, l. 5, Figs. 13, and 14).

Appellant contends the Examiner erred because the Examiner relies on a subset of outputs from the shuffle-exchange unit of Fettweis to teach or suggest the claimed *forward and inverse (N/2)-point transform computation circuit*, but "each of the outputs of such an operation is still dependent on all [N] inputs." App. Br. 8. Appellant argues an "N input, N/2 output operation

does not correspond to an '(N/2)-point transform.'" *Id.*; *see also* Reply Br. 2–4. Appellant further argues that "when operating in the IDCT mode, the shuffle-exchange circuit (30) in Fettweis receives data that has already been partially transformed. As such, the shuffle-exchange circuit (30) in Fettweis at most performs a part of an N-point transform." App. Br. 8 (citation omitted); *see also* Reply Br. 4.

Appellant also contends the Examiner erred in relying on Pan because "Pan does not include a circuit that implements" the (N/2)×(N/2) matrix multiplication relied on. App. Br. 10. Appellant argues the equation "is merely part of a derivation for [another equation] (which serves as the core component for the 2-D DCT algorithm) and is not actually implemented as a circuit in the system of Pan." *Id.*

Appellant also argues "the shuffle-exchange circuit (30) in Fettweis operates on vectors and not matrices," but "Pan operates on matrices — not vectors." *Id.*; *see also* Reply Br. 5–7. Appellant contends "replacing the shuffle-exchange circuit in Fettweis (30) with an incompatible component would not provide another way of performing the DCT and IDCT operations, but would instead destroy the functionality of the overall DCT/IDCT architecture in Fettweis, thereby rendering the system in Fettweis to be unsatisfactory for its intended purpose." App. Br. 11; *see also* Reply Br. 6–9.

Appellant makes substantially the same arguments with respect to claim 6. App. Br. 12–18; *see also* Reply Br. 9.

ANALYSIS

We agree with and adopt as our own the Examiner's findings of facts and conclusions as set forth in the Answer and in the Action from which this

appeal was taken. We have considered Appellant's arguments, but do not find them persuasive of error. We provide the following explanation for emphasis.

We are unpersuaded by Appellant's argument that an "N input, N/2 output operation does not correspond to an '(N/2)-point transform.'" App. Br. 8. As the Examiner correctly notes, "[r]egardless of how many input points [shuffle-exchange circuit] 30 comprises, [N/2] of those inputs are transformed." Ans. 3. Appellant does not identify any recitations that preclude the *forward and inverse (N/2)-point transform computation circuit* from accepting more than N/2 inputs as part of the transformation.

We are unpersuaded by Appellant's argument that "the shuffle-exchange circuit (30) in Fettweis receives data that has already been partially transformed." App. Br. 8. Appellant fails to identify recitations that proscribe the N-point input vector from having been partially transformed before being processed by the claimed apparatus.

We are unpersuaded by Appellant's arguments that "Pan does not include a circuit that implements" the (N/2)×(N/2) matrix multiplication relied on. *Id.* at 10; *see also* Reply Br. 8 ("an equation does not perform an algorithm"). "[T]he question under 35 USC 103 is not merely what the references expressly teach but what they would have *suggested* to one of ordinary skill in the art at the time the invention was made." *Merck & Co. v. Biocraft Labs., Inc.*, 874 F.2d 804, 807 (Fed. Cir. 1989) (quoting *In re Lamberti*, 545 F.2d 747, 750 (CCPA 1976)) (emphasis added). The Examiner's findings show that Pan teaches or suggests using circuitry to perform operations expressed through equations. *See* Ans. 4 (citing Pan col. 52, ll. 10–23).

We are unpersuaded by Appellant's argument that "replacing the shuffle-exchange circuit in Fettweis (30) with [Pan's] incompatible component would . . . destroy the functionality of the overall DCT/IDCT architecture in Fettweis." App. Br. 11; *see also* Reply Br. 6, 8–9. However, the test for obviousness is based on what the combined teachings of the references suggest, not on whether features of one reference can be bodily incorporated into another. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981). As the Examiner notes, the rejection does not posit replacing the entire shuffle-exchange circuit of Fettweis, but rather replacing the butterfly architecture *within* shuffle-exchange circuit 30. *See* Ans. 4 (citing Final Act. 5); *see also* Fettweis col. 6, ll. 12–21, Fig. 9 (shuffle exchange circuit 30 *employs* "butterfly units").

Finally, we are also unpersuaded by Appellant's argument that Fettweis merely operates on vectors while Pan merely operates on matrices. *See* App. Br. 10; *see also* Reply Br. 5–7. The Examiner correctly finds that a "vector is a type of matrix that . . . is one-dimensional, i.e.[,] N rows by 1 column" (Ans. 4). Appellant responds by noting "that the matrix described in Pan and relied upon by the Examiner is not an N rows by 1 column matrix." Reply Br. 5; *see also id.* at 7. Appellant's arguments are unpersuasive because an artisan of ordinary skill would have understood that the matrices described in Pan represent ordered sets of column vectors. Appellant argues that "[m]ultiplying two matrices together to produce a matrix . . . does not correspond to multiplying a vector with a matrix to produce a vector." Reply Br. 5. However, multiplying a matrix by an ordered set of column vectors (i.e., by a second input matrix) produces an output ordered set of column vectors (i.e., an output matrix). The number of

column vectors produced depends on the number of columns in the second input matrix, but the multiplication produces at least one column vector (assuming the matrices are not empty). Because an artisan of ordinary skill would have recognized and appreciated this nexus between matrices and vectors, we agree with the Examiner that the premise of Appellant's arguments—that there are major differences between vectors and matrices that would render non-obvious the use of Pan's teachings to modify Fettweis—is unsupported by the preponderance of evidence. *See* Ans. 5. Therefore, Appellant's arguments are not persuasive of error in the Examiner's findings and conclusions.

For these reasons, we agree with the Examiner that the combination of Fettweis and Pan renders obvious: (1) "a forward and inverse (N/2)-point transform computation circuit coupled to the first decomposition circuit to receive the first (N/2)-point vector"; (2) "wherein the first matrix multiplication circuit is configured to multiply the second (N/2)-point vector with an (N/2) × (N/2) matrix, the (N/2) × (N/2) matrix consisting of elements from odd lines of an N×N transform coefficient matrix"; and (3) "wherein the forward and inverse (N/2)-point transform computation circuit is configured to compute an (N/2)-point forward transform or an (N/2)-point inverse transform responsive to the control signal," as recited in claim 1.

Accordingly, we sustain the Examiner's 35 U.S.C. § 103(a) rejection of claim 1, and claim 6, which Appellant argues is patentable for substantially the same reasons. App. Br. 12–18; *see also* Reply Br. 9.

DECISION

We affirm the Examiner's decision rejecting claims 1 and 6.

In the event of further prosecution, the Examiner should ascertain whether the claims are directed to statutory subject matter. Although the Specification discloses the application of claimed forward and inverse transforms computation apparatus in HEVC, the claims contain no recitations limiting the claimed apparatus to HEVC applications. The Specification explicitly discloses that an artisan of ordinary skill would recognize "embodiments for transforms that have similar symmetry properties to the HEVC core transform." Spec. ¶ 108. Furthermore, while claimed as a combination of "circuits," the Specification broadly discloses "[e]mbodiments of the methods, encoders, and decoders described . . . may be implemented in hardware, software, firmware, or any combination thereof." Spec. ¶ 111. Thus, rather than being directed to a particular machine or being limited to particular application, the invention as claimed appears to encompass an abstract mathematical algorithm implemented on any type of machine. This Board has affirmed 35 U.S.C. § 101 rejections, or entered new grounds of rejection under 35 U.S.C. § 101, with respect to claims that are similarly directed to abstract mathematical algorithms not tied to a particular machine. *See, e.g., Ex parte Gustavson*, App. No. 2010-003918, (PTAB 2013) (expanded panel) (non-precedential), available at https://e-foia.uspto.gov/Foia/RetrievePdf?system=BPAI&flNm=fd2010003918-04-18-2013-1; *Ex parte Cryptography Research, Inc.*, App. No. 2017-005069, (PTAB 2017) (non-precedential), available at https://e-

foia.uspto.gov/Foia/RetrievePdf?system=BPAI&flNm=fd2017005069-09-26-2017-1.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

AFFIRMED