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EXAMINER
BOYLE, ABBIGALE A

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte OLIVER HAEBERLEN, KLAUS SCHIESS, and STEFAN KRAMP[1]

Appeal 2017-010251
Application 13/893,937
Technology Center 2800

Before MARK NAGUMO, RAE LYNN P. GUEST, and DEBRA L. DENNETT, *Administrative Patent Judges*.

GUEST, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF CASE

Appellant appeals[2] under 35 U.S.C. § 134(a) from the Examiner's decision to reject claims 1–14 and 21–26. *See* Examiner's Final Office Action, dated December 5, 2014 ("Final"); Examiner's Answer, dated July 14, 2017 ("Answer"). We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

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[1] The Applicant and Appellant is the real party in interest Infineon Technologies AG. *See* Appellant's Appeal Brief, dated February 22, 2017 ("App. Br.").

[2] In considering this appeal, we look to the Appellant's Appeal Brief and Reply Brief, filed July 26, 2017 ("Reply").

Appellant's invention is related to a semiconductor device and a method of making a device wherein semiconductor chips are integrated into the semiconductor device and suitable for switching or control of currents and/or voltages. Spec. 1.

Independent claim 1 is exemplary of the subject matter on appeal and is reproduced below with key limitations italicized:

> 1. A method, comprising:
>
> providing an electrically conductive carrier comprising a leadframe;
>
> placing a semiconductor chip over the carrier, the semiconductor chip having a first electrode on a first face facing the carrier;
>
> applying an electrically insulating layer over the carrier and the semiconductor chip, the electrically insulating layer having a first face facing the carrier and a second face opposite to the first face;
>
> selectively removing the electrically insulating layer; and
>
> *applying solder material* to places where the electrically insulating layer is removed and on the second face of the electrically insulating layer *such that the solder material completely fills the places where the electrically insulating layer is removed* and is on the second face of the electrically insulating layer on a first side and a second side opposite to the first side of each of the places where the electrically insulating layer is removed and extends from the first side to the second side over each of the places where the electrically insulating layer is removed *to provide an external contact element having a surface area larger than a surface area of the first electrode*.
>
> wherein a first sidewall of the electrically insulating layer is coplanar with a sidewall of the carrier and a second sidewall of the electrically insulating layer directly contacts the semiconductor chip, the second sidewall directly opposite to the first sidewall, and

> wherein the first sidewall and the second sidewall of the electrically insulating layer and the sidewall of the carrier are perpendicular to the first face.

App. Br. 11, Claim App.

The Examiner maintains the following rejections:

1. Claims 1–14 and 21–23 are rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Knapp[3] in view of Cheng,[4] Yean,[5] and Pavier;[6]
2. Claims 24–26 are rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Knapp in view of Cheng, Yean, and Pavier and further in view of Adamic.[7]

Unless otherwise indicated, we adopt the Examiner's findings in the Answer as our own and add any additional findings of fact appearing below for emphasis.

II. DISCUSSION

All of the claims under rejection will stand or fall with independent claim 1, which is representative of all of the claims on appeal.

The Examiner finds that the combined teachings of Knapp, Cheng and Yean teaches all of the steps of claim 1, but does not expressly disclose an external contact element having a surface area larger than a surface area of

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[3] US 6,835,580 B1, issued December 28, 2004, to Knapp et al. ("Knapp").
[4] US 2003/0134455 A1, published July 17, 2003, naming as inventors Cheng et al. ("Cheng").
[5] US 2004/0178495 A1, published September 16, 2004, naming as inventors Yean et al. ("Yean").
[6] US 2007/0108585 A1, published May 17, 2007, naming as inventors Pavier et al. ("Pavier").
[7] US 5,841,197, issued November 24, 1998, to Adamic, Jr. ("Adamic").

the first electrode provided. Final 5. The Examiner further finds that Pavier teaches an encapsulated chip with external contact elements (conductive pad 20) having a larger surface area than the electrode to which it is coupled "[t]o obtain the desired distribution." Final 5 (citing Pavier ¶ 18). The Examiner also notes that "Pavier reference and all four references are analogous are in that they are related to fan out packaging [FOWLP (Fan Out Wafer Level Packaging)]." Ans. 6. The Examiner notes that FOWLP are known in the art to increase distribution tolerances for increasingly densely wired chips by spreading the external connections over a greater surface area. Ans. 3. The Examiner thus determined that it would have been obvious to modify the teachings of Knapp, Cheng, and Yean to provide the external contact elements with a surface area larger than the first electrode in order to provide a desired distribution consistent with the teachings of fan out packaging. Ans. 6–7.

Appellant points out that each of the fan out packages in the prior art, including Pavier, teach "form[ing] the fan out portion of a material other than solder to provide a pad unto which solder is applied" and "none of the references teach fan out portions made of *solder*." Reply 4.

While the Examiner asserts the teachings of Pavier of larger external contact pads for improved distribution "applies to the package regardless if the contact material is copper or solder" (Ans. 4, 5), the Examiner provides no evidence to support this finding and such a finding is not supported by any of the prior art references of record. Indeed, we agree with Appellant that the fan out portions (i.e., the portions that are larger in surface area than the electrode) taught by each of Knapp, Cheng, Yean and Pavier are expressly described as metallic materials other than solder. Reply 4; *see*

Knapp col. 2, ll. 40–53, Cheng ¶ 23, Yean ¶ 26, and Pavier ¶ 18. Pavier teaches using solder only to mount contact pads 20 to onto an end user's circuit board or assembly in a similar manner taught by Knapp, Cheng, and Yean while using other materials to fan out (provide a wider surface area) the smaller size of the electrode. *See* Pavier ¶¶ 18–20. Further, Pavier, in discussing increased failure rates in solder connections when there are smaller electrodes due to electromigration or the like phenomena, appears to teach against the Examiner's finding that the materials are equivalent. Pavier ¶¶ 3–4.

Thus we are persuaded that the combination of Knapp, Cheng, Yean, and Pavier fail to suggest to one of skill in the art forming external contacts made of solder that are larger than an first electrode as recited in claim 1. Because the rejections of the remaining claims on appeal rely on the same reasoning applied to claim 1, we do not sustain the Examiner's rejections on appeal.

III. CONCLUSION

On the record before us and for the reasons discussed above, we do not sustain the Examiner's rejection of claims 1–14 and 21–23 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Knapp in view of Cheng, Yean, and Pavier and of claims 24–26 rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Knapp in view of Cheng, Yean, and Pavier and further in view of Adamic. Accordingly, we reverse the Examiner's decision to reject claims 1–14 and 21–26.

REVERSED