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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte BERND SCHAFFERER and BING ZHAO

Appeal 2017-007629
Application 14/628,730[1]
Technology Center 2600

Before DEBRA K. STEPHENS, DANIEL J. GALLIGAN, and DAVID J. CUTITTA II, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION ON APPEAL

Introduction

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1–19 and 21–23[2], which are all of the claims pending in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM IN PART.[3]

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[1] According to Appellants, the real party in interest is Analog Devices, Inc. App. Br. 4.

[2] The Examiner has withdrawn the rejection of claim 20. Ans. 18.

[3] Our Decision refers to Appellants' Appeal Brief filed November 30, 2016 ("App. Br."), Appellants' Reply Brief filed April 24, 2017 ("Reply Br."), Examiner's Answer mailed February 28, 2017 ("Ans."), Advisory Action filed December 7, 2016, and Final Office Action mailed August 2, 2016 ("Final Act.").

STATEMENT OF THE CASE

Claims on Appeal

Claims 1, 17, and 22 are independent claims. Claim 1 is reproduced below:

> 1. A high output power digital to analog converter (DAC) system, the DAC comprising:
>
> M parallel DAC cores, wherein each parallel DAC core comprises an array of current sources and a switch bank for converting most significant bits and least significant bits of a respective digital input word to a respective analog output in parallel with each other;
>
> M parallel cascodes forming a cascodes stage, wherein the M parallel cascodes are directly connected to corresponding analog outputs of M parallel DAC core via a network of traces; and
>
> a power combining network to combine output power at outputs of the M parallel cascodes to provide an aggregate analog output;
>
> wherein M is equal to or greater than two.

References

Bugeja	US 2004/0104832 A1	June 3, 2004
Huang	US 2006/0284746 A1	Dec. 21, 2006
Kaper	US 2011/0227770 A1	Sept. 22, 2011
Wyville	US 2013/0207823 A1	Aug. 15, 2013
Schafferer	US 8,970,418 B1	Mar. 3, 2015

Examiner's Rejections

Claims 1, 17, and 22 are rejected under the judicially-created doctrine of non-statutory obviousness-type double patenting over claims 1 and 7 of Schafferer. Final Act. 10–11.

Claims 10–13 stand rejected under 35 U.S.C. § 112(b) as being indefinite. *Id.* at 11–12.

Claims 1, 2, 4–9 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaper and Bugeja. *Id.* at 13–17.[4]

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaper, Bugeja, and Huang. *Id.* at 18.

Claims 14–21 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaper, Bugeja, and Wyville. *Id.* at 18–23.

ANALYSIS

Double Patenting: Claims 1, 17, and 22

Claims 1, 17, and 22 are rejected on the ground of non-statutory obviousness-type double patenting over claims 1 and 7 of Schafferer. Final Act. 11. Appellants do not challenge the merits of the double patenting rejection (*see* App. Br. 6, 12–24; *see also* Reply Br. 2–6); accordingly, we summarily sustain the Examiner's rejection of claims 1, 17, and 22.

Indefiniteness: Claims 10–13

Claims 10–13 are rejected under 35 U.S.C. § 112(b) as being indefinite. Final Act. 11–12. Appellants do not challenge the merits of the indefiniteness rejection (*see* App. Br. 6, 12–24; *see also* Reply Br. 2–6);

[4] The Final Action lists claim 3 as rejected under 35 U.S.C. § 103(a) over Kaper and Bugeja. Final Act. 13. However, the Final Action does not substantively reject claim 3 over Kaper and Bugeja (*see id.* at 13–17) and instead rejects claim 3 in a separate section over Kaper, Bugeja, and Huang (*id.* at 18). We consider the inclusion of claim 3 in the rejection over Kaper and Bugeja a typographical error.

accordingly, we summarily sustain the Examiner's rejection of claims 10–13.

We also note the Claims Appendix filed in Appellants' Appeal Brief does not accurately reflect the current language of claim 10 but instead improperly includes amendments to claim 10 (App. Br. 7) that the Examiner did not enter (Adv. Act. 2). Appellants are reminded that Appeal Briefs must comply with 37 CFR 41.37(c)(2), which prohibits the inclusion in a brief of any new or non-admitted amendment. MPEP § 1205.02.

35 U.S.C. § 103(a): Claims 1 and 17

Appellants contend the Examiner erred in finding the combination of Kaper and Bugeja teaches "parallel DAC cores, wherein each parallel DAC core comprises an array of current sources and a switch bank for converting most significant bits and least significant bits of a respective digital input word," as recited in claim 1 and similarly recited in claim 17. App. Br. 12–16; Reply Br. 2–4. Specifically, Appellants argue Figures 1A and 1B of Kaper teach "a single 'DAC core section 16.'" App. Br. 14 (emphasis omitted); Reply Br. 4. Further, Appellants argue the "DAC Least Significant Bits" (LSBs) and "DAC Most significant bits" (MSBs) components of DAC core section 16 are not "two parallel DAC cores." App. Br. 14–15; Reply Br. 3–4. According to Appellants, in Figure 3 of Kaper, "the alleged first DAC core converts ***only MSBs of the digital signal 14***, and the alleged second DAC core converts ***only LSBs of the same digital signal 14***." App. Br. 13–14; Reply Br. 3. Additionally, Appellants argue "Bugeja shows a single DAC core, and not the parallel DAC cores as claimed." App. Br. 16.

We are not persuaded. The Examiner finds, and we agree, Kaper teaches "a first DAC core (see MSBs DAC core in figure 3) and a second DAC core (see LSBs DAC core in figure 3)." Final Act. 3 (citing Kaper Fig. 3). In particular, Figure 3 of Kaper teaches the first DAC core includes "MSB DAC bit" and "MSB-1 DAC bit," i.e., MSB DAC bits, coupled to power amplifier 20a. *See* Kaper ¶ 41. Further, Figure 3 of Kaper teaches the second DAC core includes "LSB+1 DAC bit" and "LSB DAC bit," i.e., LSB DAC bits, coupled to power amplifier 20b. *See id.*

Appellants' argument that DAC core section 16 is a single DAC core, rather than a plurality of cores (App. Br. 14) does not address the Examiner's finding that DAC core section 16 includes a plurality of DAC cores, i.e., MSB DAC bits and LSB DAC bits. Final Act. 3 (citing Kaper Fig. 3).

Further, Appellants' arguments that DAC core section 16's MSB DAC bits, i.e., the first DAC core, and LSB DAC bits, i.e., the second DAC core, are not DAC cores because the "language used in Kaper" to describe those MSB and LSB DAC bits does not use the word "core" (App. Br. 14–15; Reply Br. 3) improperly suggests identity of terminology is required to reject a claim. *See In re Schaumann*, 572 F.2d 312, 317 (CCPA 1978); *see also In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). The Specification describes that "each parallel DAC core converts a digital input signal to an analog output signal." Spec. ¶ 24. Kaper's MSB DAC bits and LSB DAC bits are "individual *converter* bits of the DAC core section" (Kaper ¶ 9 (emphasis added)), i.e., those DAC bits convert received digital signals into analog signals (*see* Kaper ¶¶ 30–31, 33). Appellants also agree that "Kaper shows DAC bits . . . for converting" a digital signal. App. Br. 17. Because

Kaper's MSB DAC bits and LSB DAC bits respectively convert "a digital input signal to an analog output signal" (Spec ¶ 24), Kaper's MSB DAC bits and LSB DAC bits teach DAC cores as described by the Specification.

Furthermore, Appellants' argument that Kaper's "alleged first DAC core converts ***only MSBs of the digital signal 14***, and the alleged second DAC core converts ***only LSBs of the same digital signal 14***" (App. Br. 13–14; Reply Br. 3) is not commensurate with the scope of the claim. Initially, we note the claim recites "converting most significant bits and least significant bits" of each core's respective input word, rather than converting *the* most significant bit and *the* least significant bit, i.e., the highest-order bit and the lowest-order bit. Although it is understood that *the* most significant bit of a word is the highest-order bit and *the* least significant bit of a word is the lowest-order bit, neither the claim nor the Specification provide any definition that distinguishes which of the remaining bits in the word are "most significant bits" and which bits are "least significant bits." For example, in the word 00100111, the left-most bit '0' is the highest-order bit, and so, the most significant bit; the right-most bit '1' is the lowest-order bit, and, thus, the least significant bit; but the significance of each of the remaining middle bits "010011" is relative to other bits. As such, in Kaper's first DAC core of MSBs, the MSB-1 DAC bit is a "least significant bit" because it is a lower-order bit relative to "most significant bit" MSB DAC bit; accordingly, Kaper's first DAC core converts most significant bits and, relatively, least significant bits. Kaper, Fig. 3. It follows that, in Kaper's second DAC core of LSBs, the LSB+1 DAC bit is a "most significant bit" because it is a higher-order bit relative to "least significant bit" LSB DAC

bit; accordingly, Kaper's second DAC core also converts most significant bits and, relatively, least significant bits. *Id.*

Additionally, we are not persuaded by Appellants' argument that Bugeja does not teach parallel DAC cores (App. Br. 16) because the Examiner finds Kaper teaches parallel DAC cores. We further note, similar to Kaper, Bugeja also teaches MSB segment DAC cores and LSB segment DAC cores. Ans. 7–8 (citing Bugeja ¶¶ 5, 7, 39–40, Figs. 2, 3A).

Accordingly, we are not persuaded the Examiner fails to show the combination of Kaper and Bugeja teaches or suggests the limitations as recited in claim 1 and claim 17. Therefore, we sustain the rejection of claims 1 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Kaper and Bugeja.

35 U.S.C. § 103(a): Claims 4, 22, and 23

Appellants contend the Examiner erred in finding the combination of Kaper and Bugeja teaches "each parallel DAC core converts most significant bits and least significant bits of the same digital input word," as recited in claim 4 and similarly recited in independent claim 22. App. Br. 17. Specifically, Appellants argue "the claims require that each parallel DAC core converts both the most significant bits and the least significant bits of the same digital input word," but Kaper's DAC bits "convert[] different bits or portions of a digital input 14." *Id.* (emphasis omitted).

We are persuaded. As discussed *supra*, the Examiner finds that Kaper's first DAC core converts MSB DAC bit and MSB-1 DAC bit and Kaper's second DAC core converts LSB DAC bit and LSB+1 DAC bit. Final Act. 3 (citing Kaper, Fig. 3). However, the claim requires *each* core to

convert most significant bits and least significant bits of *the same* input word. Kaper's cores convert respective and exclusive portions of the input word (*see* Kaper ¶ 41, Figs. 2, 3), and so each core does not convert "most significant bits" and "least significant bits" of the same input word.

Accordingly, on this record, we are persuaded the Examiner erred in finding Kaper teaches the disputed limitations recited in claims 4 and 22. Furthermore, similar to Kaper, Bugeja's MSBs and LSBs only convert respective and exclusive portions of the input word, and, thus, Bugeja does not remedy Kaper's deficiencies. *See* Bueja ¶¶ 11, 32, 38, Figs. 2–3a. Therefore, we do not sustain the rejection of claims 4 and 22, as well as claim 23, which depends from claim 22, under 35 U.S.C. § 103(a) as being unpatentable over Kaper and Bugeja.

35 U.S.C. § 103(a): Claim 8

Appellants contend the Examiner erred in finding Kaper teaches "provid[ing] digital input words having bits arranged in a random manner as the respective digital input word," as recited in claim 8. App. Br. 18–20. Specifically, Appellants argue "the bits of [Kaper's] digital input signal [are] being modified by digital predistortion," which, Appellants contend, is not random. App. Br. 19.

We are persuaded. The Examiner finds Kaper teaches that "DAC system 16 [of Figure 1A] is receiving input words (see 14') having bits arranged in a random manner." Ans. 15. In Kaper, the input word, i.e., "digital signal 14'," is provided by a pre-distortion circuit that distorts a received digital signal 14 by "changing a bit or bits of the digital signal." Kaper ¶ 29, Figs. 1A, 6. We cannot readily find where Kaper teaches that

the bits of digital signal 14 are *randomly* changed to create digital signal 14'. Nor does the Examiner explain in adequate detail that Kaper's pre-distortion circuit randomly changes bits to create digital signal 14'.

Accordingly, on this record, we are persuaded the Examiner fails to show Kaper teaches or suggests the limitations as recited in claim 8. Therefore, we do not sustain the rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Kaper and Bugeja.

35 U.S.C. § 103(a): Claim 15

Appellants contend the Examiner erred in finding Kaper teaches "the digital pre-distortion processor is an open loop pre-distortion processor," as recited in claim 15. App. Br. 20–21; Reply Br. 4–5. Specifically, Appellants argue that "[o]pen loop systems as claimed do not require feedback" but that Kaper teaches a pre-distortion circuit having "a feedback path from the output of the [power amplifiers 20] back to the digital pre-distortion circuit," i.e., "a closed-loop system." App. Br. 20–21 (citing Kaper ¶¶ 34–39, Figs 1A, 1B, 6); Reply Br. 4–5.

We are persuaded. The Examiner finds Figure 6 of Kaper "does not show that pre-distortion circuit [12] is receiving any feedback signal" and, accordingly, is an open-loop pre-distortion processor. Ans. 16. Although Figure 6 does not show pre-distortion circuit 12 receiving a feedback signal, Figure 6 and its associated description do not discuss pre-distortion circuit 12 in detail. Rather, Figure 6 is focused on a single chip configuration feature. Kaper ¶¶ 43–44. The portions of Kaper that detail pre-distortion circuit 12's operation all teach that pre-distortion circuit 12 receives control signal 32 from power amplifiers 20, i.e., feedback, and, so,

is in a closed-loop system (Kaper, Figs. 1A, 1B, 4, 5, ¶¶ 32, 34, 42, claim 11). The Examiner has not sufficiently explained why, in light of Kaper's teachings that pre-distortion circuit 12 receives feedback, pre-distortion circuit 12 of Figure 6 teaches an open loop processor as claimed.

Accordingly, on this record, we are persuaded the Examiner fails to show Kaper teaches or suggests the limitations as recited in claim 15. Therefore, we do not sustain the rejection of claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Kaper, Bugeja, and Wyville.

35 U.S.C. § 103(a): Claim 18

Appellants contend the Examiner erred in finding Kaper teaches "a peak output power level of the transmitter system is at least 15 Decibel-milliwatts," as recited in claim 18. App. Br. 21–22; Reply Br. 5. Specifically, Appellants argue "[w]hile Kaper explains that a high power high dynamic range RF signal is constructed," i.e., outputted, "Kaper is silent on any peak output power level or values of the system." App. Br. 21–22 (emphases omitted); Reply Br. 5.

We are persuaded. The Examiner finds Kaper teaches outputting "a high-power analog waveform with a certain level of the dynamic range" and interprets that high-power output level to be "at least 15 Decibel-milliWatts." Ans. 17–18 (emphasis omitted) (citing Kaper ¶¶ 3, 8). Although Kaper teaches a high-power output with a certain level, we do not readily find where Kaper teaches that the certain level of that high-power output is at least 15 Decibel-milliwatts. Furthermore, the Examiner has not explained in adequate detail why Kaper's high-power output would be

understood to be at least 15 Decibel-milliwatts or why it would have been obvious that a high-power output would be at least 15 Decibel-milliwatts.

Accordingly, on this record, we are persuaded the Examiner fails to show Kaper teaches or suggests the limitations as recited in claim 18. Therefore, we do not sustain the rejection of claim 18 under 35 U.S.C. § 103(a) as being unpatentable over Kaper, Bugeja, and Wyville.

Remaining Claims 2, 3, 5–7, 9, 14, 16, 19, and 21

Appellants do not argue separate patentability for dependent claims 2, 3, 5–7, 9, 14, 16, 19, and 21, which depend directly or indirectly from claims 1 and 17. *See* App. Br. 12–24. Accordingly, for the reasons set forth above, we sustain the Examiner's decision to reject claims 2, 3, 5–7, 9, 14, 16, 19, and 21.

DECISION

We affirm the Examiner's decision rejecting claims 1, 17, and 22 under the judicially-created doctrine of non-statutory obviousness-type double patenting.

We affirm the Examiner's decision rejecting claims 10–13 under 35 U.S.C. § 112(b) as being indefinite.

We affirm the Examiner's decision rejecting claims 1, 2, 5–7, and 9 under 35 U.S.C. § 103(a) as being unpatentable over Kaper and Bugeja.

We reverse the Examiner's decision rejecting claims 4, 8, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Kaper and Bugeja.

We affirm the Examiner's decision rejecting claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Kaper, Bugeja, and Huang.

We affirm the Examiner's decision rejecting claims 14, 16, 17, 19, and 21 under 35 U.S.C. § 103(a) as being unpatentable over Kaper, Bugeja, and Wyville.

We reverse the Examiner's decision rejecting claims 15, 18, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Kaper, Bugeja, and Wyville.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

AFFIRMED-IN-PART