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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte FATMA A. SIMSEK-EGE and
NIRMAL RAMASWAMY

Appeal 2017-006420
Application 14/109,230
Technology Center 2800

Before TERRY J. OWENS, DONNA M. PRAISS, and
CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

The Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 16–24. We have jurisdiction under 35 U.S.C. § 6(b).

The Invention

The Appellants claim a NAND memory structure and a 3D NAND memory cell comprising that structure. Claim 16 is illustrative:

> 16. A NAND memory structure, comprising:
>
> a control gate material and a floating gate material disposed between a first insulating layer and a second insulating layer;
>
> a metal layer disposed between the control gate material and the floating gate material, wherein the metal layer is disposed along at least 3 sides of the floating gate material;

an interpoly dielectric (IPD) layer disposed between the metal layer and the control gate material such that the IPD layer electrically isolates the control gate material from the floating gate material, wherein the IPD layer is disposed along at least 3 sides of the metal layer; and

optionally, a tunnel dielectric material coupled to the floating gate material opposite the control gate material.

The References

Yasuda	US 2007/0132004 A1	June 14, 2007
Alsmeier	US 2012/0001252 A1	Jan. 5, 2012
Lu	US 2013/0001667 A1	Jan. 3, 2013

The Rejections

The claims stand rejected under 35 U.S.C. § 103 as follows: claims 16–23 over Alsmeier in view of Yasuda and claim 24 over Alsmeier in view of Yasuda and Lu.

OPINION

We reverse the rejections. We need address only the broadest claim, i.e., independent claim 16.[1] That claim requires a metal layer which is between a control gate material and a floating gate material and is disposed along at least 3 sides of the floating gate material.

Alsmeier discloses a NAND memory structure comprising a dielectric layer (blocking dielectric 7) which is between a control gate electrode (3) and a floating gate (discrete charge storage segment 9) and is disposed along at least 3 sides of the floating gate (9) (¶¶ 43, 44, 46; Fig. 1A). The control

[1] The Examiner does not rely upon Lu for any disclosure that remedies the deficiency in Alsmeier and Yasuda as to the limitations in claim 16 (Final Act. 6–7).

gate electrode (3)'s sides and the dielectric layer (7)'s outer sides are adjacent to insulating material (122 a, b) (¶¶ 51, 52; Fig. 9).

Yasuda discloses a NAND memory structure comprising, in order, a control gate (CG), an inter-polysilicon dielectric (IPD), a large-work-function material, and a floating gate electrode (FG) (¶¶ 61, 63; Fig. 8). The large-work-function material, which can be metal, reduces current leakage from the floating gate electrode (FG) to the control gate electrode (CG) when an electric charge is injected into the floating gate electrode (FG) during programming (¶¶ 84, 85).

The Examiner finds that Alsmeier's floating gate (9) can be metal or polysilicon (¶ 49) and that, therefore, one of ordinary skill in the art, in view of Yasuda, would have made Alsmeier's floating gate (9) such that it has a metal portion between a polysilicon portion and the dielectric layer (7) "to reduce leakage, reduce program time and enhance performance of the NAND memory" (Final Act. 4), and because Alsmeier's floating gate (9) is formed by atomic layer deposition (ALD) or chemical vapor deposition (CVD), the metal necessarily would coat all of the dielectric layer (7)'s exposed surfaces, i.e., the end and inner walls, such that the dielectric layer (7) would be disposed on at least 3 sides of the metal portion, and after the polysilicon portion has been deposited within the metal portion, the metal portion would be disposed on at least 3 sides of the polysilicon portion (Ans. 2–7).

Setting forth a prima facie case of obviousness requires establishing that the applied prior art would have provided one of ordinary skill in the art with an apparent reason to modify the prior art to arrive at the claimed invention. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

The Examiner does not establish that the applied references would have provided one of ordinary skill in the art with an apparent reason to deposit or leave Yasuda's metal layer on Alsmeier's dielectric layer (7)'s inner sidewalls. Yasuda indicates that Yasuda's metal layer would reduce electric charge transfer from Alsmeier's floating gate (9) to the control gate electrode (3) when electric charge is injected into the floating gate (9) during programming (¶ 84), but only the end of Alsmeier's floating gate (9) faces the control gate electrode (3) (Fig. 1A). The Examiner does not establish that Yasuda's metal layer on Alsmeier's dielectric layer (7)'s inner sidewalls would contribute to that electric charge transfer reduction.

Thus, the Examiner has not established a prima facie case of obviousness of the Appellants' claimed NAND memory structure.[2]

DECISION/ORDER

The rejections under 35 U.S.C. § 103 of claims 16–23 over Alsmeier in view of Yasuda and claim 24 over Alsmeier in view of Yasuda and Lu are reversed.

It is ordered that the Examiner's decision is reversed.

REVERSED

[2] The Appellants' metal layer disposed along at least 3 sides of the floating gate material is the residual of a metal layer (420) applied beneath floating gate material (422) to enable more aggressive etching of the floating gate material, particularly at the bottom of a cell pillar trench (405), to eliminate all or substantially all debris and residual defects and to increase the process margin gain (Spec. 9:17–29, 11:16–19; Figs. 4A–C).