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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte KOJI NII,
MAKOTO YABUUCHI, YASUMASA TSUKAMOTO,
and KENGO MASUDA

Appeal 2017-005861
Application 14/236,067
Technology Center 2800

Before ADRIENE LEPIANE HANLON, GEORGE C. BEST,
and MICHAEL G. McMANUS, *Administrative Patent Judges*.

McMANUS, *Administrative Patent Judge.*

DECISION ON APPEAL

The Examiner finally rejected claims 1, 2, and 25 of Application 14/236,067 under 35 U.S.C. § 103(a) as obvious. Final Act. 2–9 (Feb. 22, 2016). Appellants[1] seek reversal of these rejections pursuant to 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6.

For the reasons set forth below, we REVERSE.

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[1] Renesas Electronics Corporation is identified as the real party in interest. Appeal Br. 1.

BACKGROUND

The present application generally relates to a semiconductor device having a static random access memory (SRAM) memory cell. Spec. 1. In a typical SRAM memory cell having six transistors, a drive transistor is connected between a storage node and a ground potential and an access transistor is connected between the storage node and a bit line. *Id.* The application indicates that, when reading data, it is necessary to increase a threshold voltage of the access transistor and attain a high ratio of drive transistor current to access transistor current to secure a read margin. Conversely, when writing data, the threshold voltage of the access transistor must be decreased in order to attain a high ratio of access transistor current to load transistor current in order to secure a write margin. *Id.* at 2–3. The application indicates that an access transistor having a pair of halo regions with asymmetric impurity concentrations may be used to adjust the threshold transistor's voltage. *Id.* at 2.

Claim 1 is representative of the pending claims and is reproduced below:

> 1. A semiconductor device having a static random access memory, comprising:
>
> a storage node including a first storage node and a second storage node storing data;
>
> a pair of bit lines sending/receiving data;
>
> a ground interconnection to which a ground potential is applied;
>
> a first element formation region and a second element formation region, each of which is defined by an element isolation insulation film in a predetermined region of a main surface of a semiconductor substrate;

an access transistor formed in said first element formation region and including a first source-drain region and a second source-drain region that are spaced away from each other and have first conductivity type, said access transistor including an access gate electrode positioned above a region interposed between said first source-drain region and said second source-drain region; and

a drive transistor formed in said first element formation region and including a third source-drain region and a fourth source-drain region that are spaced away from each other and have the first conductivity type, said drive transistor including a drive gate electrode positioned above a region interposed between said third source-drain region and said fourth source-drain region,

said access transistor including

a first halo region having a first impurity concentration and second conductivity type, said first halo region being formed in a region just below said access gate electrode so as to be adjacent to said first source-drain region electrically connected to a predetermined bit line of said pair of bit lines, and

a second halo region having a second impurity concentration and the second conductivity type, said second halo region being formed in the region just below said access gate electrode so as to be adjacent to said second source-drain region electrically connected to said storage node,

said drive transistor including

a third halo region having a third impurity concentration and the second conductivity type, said third halo region being formed in a region just below said drive gate electrode so as to be adjacent to said third source-drain region electrically connected to said storage node, and

a fourth halo region having a fourth impurity concentration and the second conductivity type, said fourth halo region being formed in the region just below said drive gate

electrode so as to be adjacent to said fourth source-drain region electrically connected to said ground interconnection,

said second impurity concentration being higher than said first impurity concentration,

said third impurity concentration being higher than said fourth impurity concentration,

said first impurity concentration and said fourth impurity concentration being set to be different impurity concentrations.

Appeal Br. 10–11 (Claims App.).

REJECTIONS

On appeal, the Examiner maintains the following rejections:

1. Claims 1 and 2 are rejected under 35 U.S.C. § 103(a) as obvious over Zhu[2] in view of Ieong[3]. Final Act. 3–7.
2. Claim 25 is rejected under 35 U.S.C. § 103(a) as obvious over Zhu in view of Ieong and further in view of Liaw[4] and Chan[5]. *Id.* at 8–9.

DISCUSSION

Rejection 1. The Examiner rejected claims 1 and 2 over Zhu in view of Ieong. *Id.* at 3–7. We select claim 1 as representative. In support of the rejection, the Examiner found that Zhu teaches an SRAM memory cell having the claimed second halo region and third halo region. *Id.* at 5. The

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[2] US 2009/0218631 A1, published Sept. 3, 2009.
[3] US 6,466,489 B1, issued Oct. 15, 2002.
[4] US 2010/0259971 A1, published Oct. 14, 2010.
[5] US 2005/0073874 A1, published Apr. 7, 2005.

Examiner further found that Zhu does not teach the first or fourth halo regions nor the claimed relative concentrations of the halo regions. *Id.*

The Examiner further found that Ieong teaches a first halo region, and a fourth halo region. *Id.* at 6. The Examiner also found that Ieong teaches that the second impurity concentration is higher than the first impurity concentration and the third impurity concentration is higher than the fourth. *Id.* The Examiner additionally determined that neither Zhu nor Ieong teach the first impurity concentration differing from the fourth but that such feature "is likely the product not of innovation but of ordinary skill and common sense." *Id.* at 7. Appellants argue that the rejection is in error on two bases.

First, Appellants argue that the rejection is in error regarding the concentration relationships shown by Ieong. Appeal Br. 6–8. Appellants assert that the Examiner conflates the first and second halo regions. The Examiner relies, in part, on Figure 8D of Ieong reproduced below:

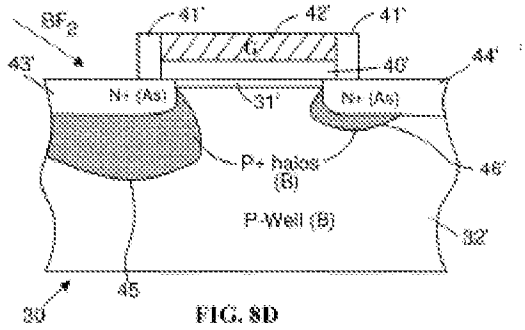

FIG. 8D

(Figure 8D is a schematic sectional view showing one stage in the process for forming a NMOS FET device. Ieong 6:58–62.) The Examiner finds that halo region 46' (on the right side of the diagram) is the "first halo region." Final Act. 6.

Claim 1 requires that the first halo region is "adjacent to said first source-drain region electrically connected to a predetermined bit line." Appellants look to Figure 8E, reproduced below, for its description of the location of the source and drain.

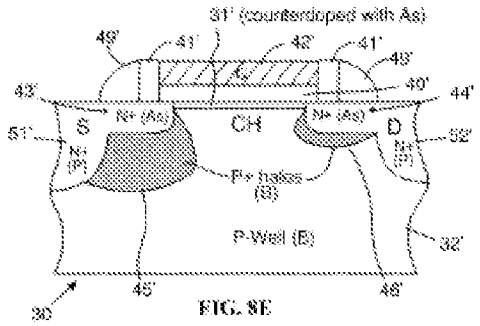

FIG. 8E

(Figure 8E is a schematic sectional view showing a stage in the process for forming a NMOS FET device subsequent to that depicted by Figure 8D.) Here, one can see that the left side is marked "S" for source and the right side marked "D" for drain. *See also* Ieong 14:23–25 ("the source region **43'** on the left and the drain region **44'** on the right."). Thus, the structure that the Examiner designates as the first halo region (46′) is on the drain side.

Appellants additionally refer to Ieong's Figure 5B, reproduced below, which shows a circuit in keeping with the invention:

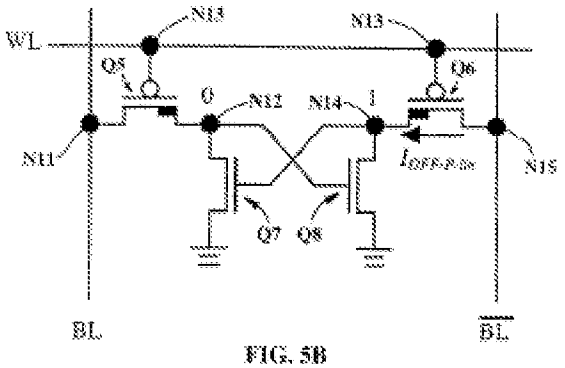

FIG. 5B

(Fig. 5B is a schematic diagram of an SRAM MOSFET circuit.) Appellants argue that Ieong teaches that the *drain* of transistor Q5 (in Figure 5B) is

connected to node 12. Appeal Br. 7 (citing Ieong 11:35–37 ("[t]he drain electrode of Super Halo asymmetric pass transistor Q5 and the drain electrode of pull down transistor Q7 are connected through node 12"). Ieong further provides that "[t]he *source* of Super Halo asymmetric pass transistor Q5 is connected to bit line BL-bar."[6] Ieong 11:31–33 (emphasis added). Thus, Ieong's specification indicates that the source of the transistor is on the bit line side and the drain on the storage node side. Accordingly, halo region 46′ of Figures 8D and 8E may be characterized as the second halo region (on the storage node side) but not as the first halo region (on the bit line side).

In the Answer, the Examiner refers to Figure 4 of Zhu which depicts an asymmetrical access transistor having a halo region on the storage node side and no halo on the bit line side. Answer 4 (citing Zhu ¶¶ 40–41; Fig. 4). The Examiner determines that the "halo region on the Bit line (15) side is mapped as first halo region and the halo region on the storage node (11) side is mapped as second halo region." *Id.* The Examiner further determines that, "[a]s there [are] some halo materials exist[ing] in second halo region, and no/zero halo materials exist in the first halo region, the limitation '*said second impurity concentration being higher than said first impurity concentration*' is met." *Id.* Finally the Examiner concludes "Zhu et al. teach the connection of the source/drain having different concentration of halo regions between the storage node and the bit line node. Secondary art,

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[6] We note that the Specification indicates that the source is connected to the bit line at "node N9." Ieong 11:33. As node N9 does not appear in Figure 5B, the reference appears to be in error.

[I]eong et al. is used only to replace the asymmetrical transistor of Zhu et al., NOT how to connect." *Id.*

This, however, differs from the Examiner's earlier finding that Zhu does not teach the "second impurity concentration being higher than said first impurity concentration." Final Act. 5.

Here, it is undisputed that Zhu does not teach a first halo region (on the bit line side). *See* Zhu Fig. 4. Accordingly, Zhu does not teach the relative concentrations of the first and second halo regions. Moreover, the Examiner supplies no reason as to why a person of ordinary skill in the art would have been motivated to disregard the source/drain arrangement as taught by Ieong. Accordingly, Appellants have shown reversible error in the Examiner's findings regarding the references' disclosure of the claimed relationship of the concentrations of the first and second halo regions.

Second, Appellants argue that the Examiner erred by finding that the claimed impurity concentration relationship between the first and fourth halo regions was not novel. Appeal Br. 8. The Examiner determined that, where there is a design need or market pressure to solve a problem and there are a finite number of solutions, one has good reason to pursue the known options and that any resulting product is likely the result of ordinary skill and common sense. Final Act. 7. In the Answer, the Examiner additionally stated that the two halo regions will have different concentrations as a result of "natural process variation" in the manufacturing process. Answer 5–6.

Appellants argue that the Examiner makes only a "bare assertion" that the claimed relationship is within the prior art and not novel. Appeal Br. 8. Appellants argue that such assertion is inadequate to support a finding of obviousness.

"Common sense has long been recognized to inform the analysis of obviousness if explained with sufficient reasoning." *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1328 (Fed. Cir. 2009). Here, however, there is little explanation of the prior art, any design need or market pressure, and whether there are, in fact, a finite number of solutions. In such a case, a finding of absence of novelty based on common sense is unsupported. *See In re Zurko*, 258 F.3d 1379, 1383–85 (Fed. Cir. 2001) (reversing Board where it adopted examiner's unsupported assertion that claim limitation missing from cited references was "basic knowledge" and it "would have been nothing more than good common sense" to combine the references).

In addition, we construe the term "different" in the clause "said first impurity concentration and said fourth impurity concentration being set to be different impurity concentrations" to require a difference beyond that slight process variation that is typical in the industry. Answer 6. The Examiner has not shown that the first impurity concentration and fourth impurity concentration are "different" under this construction.

Accordingly, Appellants have shown reversible error in the Examiner's findings regarding the finding of absence of novelty of the claimed relationship of the impurity concentrations of the first and fourth halo regions.

In view of the foregoing, we reverse the rejection of claims 1 and 2.

Rejection 2. The Examiner rejected claim 25 as obvious over Zhu in view of Ieong and further in view of Liaw and Chan. Final Act. 8–9. Claim 25 depends from claim 1. Appeal Br. 11 (Claims App.) Appellants rely upon the same arguments in regard to claim 25 as with regard to claims 1

and 2. Appeal Br. 9. The Examiner has not relied on the additional prior art of record (here, Liaw and Chan) to cure the deficiencies Zhu and Ieong identified in regard to the first rejection. Final Act. 8–9. As we have found Appellants' arguments to be persuasive with regard to claims 1 and 2, we similarly determine such arguments to require the reversal of the rejection of claim 25.

CONCLUSION

The rejection of claims 1 and 2 as obvious over Zhu in view of Ieong is reversed. The rejection of claim 25 as obvious over Zhu in view of Ieong and further in view of Liaw and Chan is reversed.

REVERSED