UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/191,282	07/26/2011	Claudio Adragna	853063.597	3787

38106 7590 02/04/2019

Seed IP Law Group LLP/ST (EP ORIGINATING)
701 FIFTH AVENUE, SUITE 5400
SEATTLE, WA 98104-7092

EXAMINER
RIVERA-PEREZ, CARLOS O

ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
02/04/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOeAction@SeedIP.com
pairlinkdktg@seedip.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL
AND APPEAL BOARD

Ex parte CLAUDIO ADRAGNA

Appeal 2017-005698
Application 13/191,282
Technology Center 2800

Before MICHAEL P. COLAIANNI, GEORGIANNA W. BRADEN, and SHELDON M. McGEE, *Administrative Patent Judges*.

COLAIANNI, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134 the final rejection of claims 1–6, 8–10, 12–15, 17–20, and 22. We have jurisdiction over the appeal pursuant to 35 U.S.C. § 6(b).

We REVERSE.

The invention is directed to a control device of a switching power supply. (claim 1; Spec. 1).

Claim 1 is illustrative:

> 1. A control device for controlling a switching converter that includes a switch, said control device comprising:
> a zero crossing detector configured to:
> receive from the switching converter an input signal,
> detect a first zero crossing of said input signal that occurs after the switch is turned off and while the switch is off,
> detect a second zero crossing immediately following the first zero crossing and occurring in an opposite direction with respect to the first zero crossing, the second zero crossing occurring in a same switching cycle of the switch as the first zero crossing, and
> output a detection signal in response to detecting said second zero crossing; and
> a synchronizer configured to start an on time period of the switch in response to the detection signal indicating that the zero crossing detector has detected said second zero crossing of said input signal.

Appellant appeals the following rejections:

1. Claims 1, 8, 9, 17, 18, and 22 are rejected under 35 U.S.C. § 102(b) as unpatentable over Yamada (US 6,842,353 B2, Jan. 11, 2005).

2. Claims 2–6, 10, 12–15, 19, and 20 are rejected under 35 U.S.C.

[1] According to the Appeal Brief, the real party in interest is listed as "STMicroelectronics S.r.l." (App. Br. 2).

§ 103 as unpatentable over Yamada in view of Pidutti (US 2004/0095101 A1, May 20, 2004).

FINDINGS OF FACT & ANALYSIS

Claim 1 is directed to a control device comprising, in relevant part, "a zero crossing detector configured to: . . . detect a first zero crossing of said input signal that occurs after the switch is turned off and while the switch is off, detect a second zero crossing immediately following the first zero crossing and occurring in an opposite direction with respect to the first zero crossing, the second zero crossing occurring in a same switching cycle of the switch as the first zero crossing, ..."

The Examiner finds that Yamada anticipates this limitation in Figure 7 (Final Act. 3). The Examiner finds that Yamada's Figure 7 shows a first zero crossing is detected after the switch 13 is turned off during a time prior to time t2 (Final Act. 3). The Examiner finds that Yamada teaches that at time t2 the switch is turned off during detection of a zero-crossing (Final Act. 3). The Examiner determines that the broadest reasonable interpretation of the claim language encompasses Yamada's first zero crossing as shown at time t2 in curve $B(I_L)$ of Figure 7 which occurs after the switch 13 is turned off during a prior time period between time t0 and t1 (Ans. 4). The Examiner determines that at time t2 the switch 13 is turned off because the Vg1 voltage goes low in Figure 7 and therefore the first zero crossing occurs while the switch is off (Ans. 4). The Examiner finds that in Yamada's Figure 7, curve $B(I_L)$ at time t2 shows that the second zero crossing occurs in the same switching cycle of the switch (Final Act. 3).

Appellant argues that Figure 7 of Yamada shows that the second peak at time t2 of the I_L waveform occurs simultaneously with the high-low

transition in the Vg1 waveform (Reply Br. 2). Appellant contends that if the Examiner is correct that a zero-crossing in the signal 36 occurs at the second peak in the I_L waveform at time t2, that means that the zero-crossing in the signal 36 at best occurs simultaneously with the high-low transition in the Vg1 waveform (Reply Br. 2). Appellant contends that one of ordinary skill in the art would understand that the switch 13 turns off at a very short time after the high-low transition in the Vg1 waveform (Reply Br. 2). Appellant argues that the zero-crossing in the signal 36 at time t2 does not occur after the switch 13 turns off and while the switch is off as required by claim 1 (Reply Br. 2; App. Br. 18).

We begin our analysis by construing the disputed claim language in light of the Specification. *In re Academy of Science Tech. Ctrs.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) ("During examination, "claims . . . are to be given their broadest reasonable interpretation consistent with the specification, and . . . claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art."). Claim 1 recites that the zero crossing detector is configured to detect a first zero crossing of the input signal that occurs *after the switch is turned off and while the switch is off*. The zero crossing detector detects the second zero crossing immediately following the first zero crossing and occurring in the opposite direction with respect to the first zero crossing, the second zero crossing occurring in the same switching cycle of the switch as the first zero crossing. Claim 1 plainly requires that the first zero crossing detection occurs after and while the switch is turned off and the first and second zero crossing detections occur as part of the same switching cycle. The Specification discloses that the switching cycle, Tsw, spans the period of

time from when the switch is on to when the switch is turned off and then the switch is turned back on (Spec. 11; Figs. 2, 4, 6; Vgs). The Specification describes that the first zero crossing, Z1, is detected after the switch was turned off for a period of time and while the switch is turned off (i.e., the Vgs voltage is zero in the Vgs curve) (Figure 2, 4, 6, Z1, Vgs) during the same switching cycle Tsw that the second zero crossing is detected. In other words, the claim as read in light of the Specification requires that the zero crossing detector is configured so that it detects the first zero crossing after and while the switch is turned off for a period of time for the same switching cycle where the detector detects the second zero crossing.

With this claim construction in mind, the Examiner has not shown within the meaning of 35 U.S.C. § 102 that Yamada teaches the disputed claim subject matter. The Examiner finds that Yamada's disclosure to detect a first zero crossing at time t2 after the switch is turned off during the time period of t0 to t1 would satisfy the claim. At time t2, however, Yamada's zero crossing appears to be detected simultaneously with the turning off the switch 13 (i.e., Vgs goes low in Yamada's Figure 7; Yamada col. 8, ll. 45-46). The Specification describes that the detection of the first zero crossing occurs after and during the time that the switch is off of the same switching cycle that the second zero crossing is detected. *See e.g.*, Fig. 4, Z1, Z2, Vgs. The Examiner has not directed us to where the Specification supports the Examiner's claim construction that includes where Yamada's switch is turned off during an earlier switch cycle (i.e., during time t0 and t1) and then the switch is turned on and shut down at time t2 while simultaneously detecting a first zero crossing.

On this record, we are constrained to reverse the Examiner's § 102(b) rejection of claims 1, 8, 9, 17, 18, and 22. The Examiner's § 103 rejection of dependent claims 2–6, 10, 12–15, 19, and 20 over Yamada in view of Pidutti does not cure the deficiencies discussed above with respect to the § 102(b) rejection over Yamada alone. Therefore, we reverse the Examiner's rejections of record.

DECISION

The Examiner's decision is reversed.

ORDER

REVERSED