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PVF -- SYNOPSYS, INC
c/o PARK, VAUGHAN, FLEMING & DOWLER LLP
2820 FIFTH STREET
DAVIS, CA 95618-7759

EXAMINER
LEE, ERIC D

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jeannie@parklegal.com
wendy@parklegal.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte AMIR H. MOTTAEZ and MAHESH A. IYER

Appeal 2017-004758
Application 14/016,010
Technology Center 2800

Before GEORGE C. BEST, MONTÉ T. SQUIRE, and MERRELL C. CASHION, JR., *Administrative Patent Judges*.

SQUIRE, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

Appellant[2] appeals under 35 U.S.C. § 134(a) from the Examiner's decision to reject claims 1–12 and 17–22, which constitute all the claims pending in this application. 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

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[1] In explaining our Decision, we refer to the Specification filed August 30, 2013 ("Spec."); Final Office Action dated July 30, 2015 ("Final Act."); Appeal Brief filed April 29, 2016 ("Appeal Br."); Examiner's Answer dated November 25, 2016 ("Ans."); and Reply Brief filed January 25, 2017 ("Reply Br.").

[2] Appellant is the Applicant, Synopsys, Inc., which is also identified as the real party in interest. Appeal Br. 3.

We AFFIRM.

The Claimed Invention

The claimed subject matter relates to electronic design automation (EDA) software tools for use in circuit synthesis and design and, in particular, to a method for discretizing cell/gate sizes during numerical synthesis. Spec. Abstract, ¶¶ 2, 23, 24.

Claim 1 is illustrative of the claimed subject matter on appeal and is reproduced below from the Claims Appendix to the Appeal Brief (Appeal Br. 23):

> 1. In an electronic design automation (EDA) software tool in a computer, a method for discretizing cell sizes during numerical synthesis, the method comprising:
>
> ***the EDA tool in the computer receiving an optimal input capacitance value for an input of an optimizable cell***, wherein the input of the optimizable cell is driven by an output of a driver cell, and wherein the input capacitance value is determined by a numerical solver in the computer that is optimizing a circuit design for best delay;
>
> the EDA tool in the computer identifying a first library cell whose input capacitance value is closest to the optimal input capacitance value, wherein the first library cell is selected from a technology library;
>
> ***the EDA tool in the computer computing a delay from an input of the driver cell to an output of the optimizable cell*** assuming the first library cell is instantiated at the optimizable cell; and
>
> the EDA tool in the computer identifying a second library cell from the technology library, wherein the input capacitance value of the second library cell is less than or equal to the input capacitance value of the first library cell, and wherein instantiating the second library cell at the optimizable cell

would improve the delay from the input of the driver cell to the output of the optimizable cell.

The References

The Examiner relies on the following prior art references as evidence in rejecting the claims on appeal:

Scott et al., (hereinafter "Scott")	US 2005/0081175 A1	Apr. 14, 2005
Morgenshtein et al., (hereinafter "Morgenshtein")	US 2009/0150847 A1	June 11, 2009

The Rejections

On appeal, the Examiner maintains (Ans. 2) the following rejections:

1. Claims 1–12 and 17–22 rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter ("Rejection 1"). Final Act. 3.

2. Claims 1–12 and 17–22 rejected under 35 U.S.C. § 103 as being unpatentable over Morgenshtein in view of Scott ("Rejection 2"). Final Act. 4.

OPINION

Having considered the respective positions advanced by the Examiner and Appellant in light of this appeal record, we affirm the Examiner's rejections based on the fact finding and reasoning set forth in the Answer and Final Office Action, which we adopt as our own. We highlight and address specific findings and arguments below for emphasis.

Rejection 1

Appellant argues independent claims 1–12 and 17–22 as a group. Appeal Br. 13. We select claim 1 as representative and the remaining claims subject to the Examiner's rejection stand or fall with claim 1. 37 C.F.R. § 41.37(c)(1)(iv).

The Examiner determines that Appellant's claimed invention is unpatentable under 35 U.S.C. § 101 because it is directed to non-statutory subject matter. Final Act. 3–4; *see also* Ans. 2–9. In particular, the Examiner determines that:

> [T]he claims are directed to the abstract idea of a mathematical relationship/algorithm for receiving an optimal input capacitance, identifying a first library cell whose input capacitance is closest to the optimal input capacitance, computing a delay, and identifying a second library cell having less than or equal to input capacitance to the first library cell.

Final Act. 3; *see also* Ans. 2–8.

The Examiner further determines that the additional elements or combination of elements recited in the claims other than the abstract idea amount to no more than "mere instructions to implement the idea on a computer" and do not "transform the abstract idea into a patent-eligible subject matter." Final Act. 3 (citing *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 134 S. Ct. 2347, 2358 (2014)); *see also* Ans. 8; *Elec. Power Grp. v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016)).

Appellant argues that the Examiner's rejection should be reversed because the rejection "does not include any 'comparison' of the alleged abstract idea in the independent claims with the 'concepts already found to be abstract' in *Alice Corp.*" Appeal Br. 13 (citing the July 2015 Update on

Subject Matter Eligibility[3]). Appellant contends that the Examiner "fails to properly state a § 101 rejection in accordance with the instructions that were specified in the July 2015 Update." *Id.* at 13–14.

Appellant further argues that the claims are not directed to any of the four categories of abstract ideas provided in the July 2015 Update. *Id.* at 16. In particular, Appellant contends that

> the claimed subject matter clearly does not fall into any of the abstract idea categories because (1) it does not relate to the economy or commerce, therefore it is not a fundamental economic practice, (2) it does not relate to interpersonal and intrapersonal activities, therefore it is not a certain method of organizing human activity, (3) it is not an uninstantiated concept, plan, or scheme, and (4) it is not a mathematical algorithm, relationship, formula, or calculation.

Id. at 17.

Appellant also argues that the Examiner is "grossly oversimplifying" the claimed subject matter and the claims are "not directed to an abstract idea based on *Alice*." Appeal Br. 14. In particular, Appellant contends that the claims are distinguishable from the claims found ineligible in *Alice* because, unlike the claims in *Alice*, they are not directed to the abstract idea of "employing an intermediary to facilitate simultaneous exchange of obligations in order to minimize risk." *Id.* at 14–15.

Appellant argues that the claims are patent eligible under *Alice* because they "improve another technology, namely, the technology of circuit design and manufacturing." *Id.* at 17. Appellant contends that, just like the

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[3] July 2015 Update on Subject Matter Eligibility, 80 Fed. Reg. 45429 (published July 30, 2015) ("July 2015 Update").

claims found patentable in *McRO*, claim 1 is directed to achieve an improved technological result because it "results in an improved numerical synthesis process that uses an improved way for discretizing cell sizes." Reply Br. 9 (citing *McRO, Inc. v. Bandai Namco Games Am. Inc.*, 837 F.3d 1299, 1314 (Fed. Cir. 2016)).

We do not find Appellant's arguments persuasive of reversible error in the Examiner's rejection.

The Supreme Court's decision in *Alice* identifies a two-step framework for determining whether claimed subject matter is judicially-excepted from patent eligibility under § 101. According to *Alice* step one, "[w]e must first determine whether the claims at issue are directed to a patent-ineligible concept," such as an abstract idea. *Alice*, 134 S. Ct. at 2355.

Step two of the *Alice* framework is "a search for an 'inventive concept'—*i.e.,* an element or combination of elements that is 'sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the [ineligible concept] itself.'" *Id.* at 2355 (quoting *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S. 66, 72 (2012)). In applying step two, we must determine whether there are any "additional features" in the claims that constitute an "inventive concept," *Alice*, 134 S. Ct. at 2357, and whether those "additional features" amount to more than merely "well-understood, routine, conventional activity." *Mayo*, 566 U.S at 79.

Beginning with the first step of the *Alice* framework, we look at claim 1 to determine whether it is directed to an abstract idea. Claim 1 recites a method comprising the following steps performed via "the EDA

tool in the computer": (1) "receiving an optimal input capacitance value for an input of an optimizable cell"; (2) "identifying a first library cell whose input capacitance value is closest to the optimal input capacitance value"; (3) "computing a delay from an input of the driver cell to an output of the optimizable cell"; and (4) "identifying a second library cell from the technology library." Appeal Br. 23 (Claims App'x).

Based on the claim's language, the Specification, and a preponderance of the evidence of record before us, we concur with the Examiner's determination that claim 1 is directed to the abstract idea of a mathematical relationship/algorithm. In particular, based on the Examiner's fact-finding and well-stated reasoning provided at pages 3–8 of the Answer and pages 3–4 of the Final Office Action, we determine that each of the recited steps of claim 1 is directed to and uses a mathematical algorithm for performing calculations and mathematically manipulating and/or comparing data. *See* Spec. ¶¶ 32, 39, 41, 44, 50, 58, 62.

For example, as the Examiner finds (Ans. 3), the step of "receiving an optimal input capacitance value for an input of an optimizable cell" (step (1) enumerated above) involves solving a mathematical equation in order to generate a mathematical value used in the next step of the mathematical algorithm. Indeed, this claim step explicitly recites that "the input capacitance value is determined by a numerical solver in the computer that is optimizing a circuit design for best delay." Appeal Br. 23 (Claim App'x).

As the Examiner explains (Ans. 4), the "optimal input capacitance value" is calculated by solving mathematical equations based on numerical delay models. Spec. ¶ 32 (disclosing that "an analytical formula that represents the delay behavior is an example of a numerical delay model"),

¶ 39 (disclosing numerical synthesis using "numerical delay models" and that the output includes the "numerically optimized . . . input capacitance value"), ¶ 41 ("Output 116 is then provided as one of the inputs to the second phase of numerical synthesis (discretization) 118.").

As the Examiner further explains (Ans. 7), the step of "computing a delay from an input of the driver cell to an output of the optimizable cell" (step (3) enumerated above) explicitly uses a mathematical algorithm to "compute" the delay based on operations performed by the computer. Spec. ¶ 50 (disclosing that the "computer can then iterate through each library cell" and "compute a slack value").

The fact that the mathematical algorithm relates to circuit design software and a method for discretizing cell/gate sizes during numerical synthesis, as opposed to some business method, and the claimed method may be implemented using generic computer equipment (i.e., via "the EDA tool in the computer") does not render the claim patent-eligible or the underlying idea any less abstract. *See Alice*, 134 S. Ct. at 2358 (holding that "the mere recitation of a generic computer cannot transform a patent-ineligible abstract idea into a patent-eligible invention"); *see also Fair Warning IP, LLC v. Iatric Sys., Inc.*, 839 F.3d 1089, 1095 (Fed. Cir. 2016) (citing *Bancorp Servs., LLC v. Sun Life Assurance Co.*, 687 F.3d 1266, 1278 (Fed. Cir. 2012) ("[T]he fact that the required calculations could be performed more efficiently via a computer does not materially alter the patent eligibility of the claimed subject matter.")).

Moreover, we concur with the Examiner that the claims are similar to claims found to be patent-ineligible in prior cases for being directed to the abstract idea of mathematical relationships/algorithms. Ans. 7–8 (citing

Gottschalk v. Benson, 409 U.S. 63 (1972) and *In re Grams*, 888 F.2d 835 as exemplary cases).

Appellant's argument regarding the *McRO* decision (Reply Br. 9) is not persuasive because the instant claims are distinguishable from the claims at issue in that case. In *McRO*, the court found that the claims were not abstract because they were "focused on a specific asserted improvement in computer animation." *McRO*, 837 F.3d at 1314. In particular, the court found that the claims in *McRO* were directed to the creation of something physical—namely, the display of "lip synchronization and facial expressions" of animated characters on screens for viewing by human eyes and the claimed improvement was to how the physical display operated to produce better quality images. *Id.* at 1313–14.

Here, unlike the claims found non-abstract in *McRO*, Appellant's claimed invention is directed to a mathematical algorithm for performing calculations and mathematically manipulating and/or comparing data, and does not recite an improvement to a particular computer technology in the physical sense as was the case in *McRO*.

Because the steps of claim 1 each principally involves solving mathematical equations and/or performing computations using numerical delay models, they could each conceivably be performed using mental steps, pen, and paper. *See Intellectual Ventures I LLC v. Symantec Corp.*, 838 F.3d 1307, 1318 (Fed. Cir. 2016) (claims directed to an abstract idea, where "with the exception of generic computer-implemented steps, there is nothing in the claims themselves that foreclose them from being performed by a human, mentally or with pen and paper"); *see also Elec. Power Grp.*, 830 F.3d at 1354 (treating "analyzing information by steps people go through in their

minds, or by mathematical algorithms, without more, as essentially mental processes within the abstract-idea category").

Turning to the second step of *Alice*, on the record before us, we determine that claim 1 does not contain an inventive concept sufficient to transform the nature of the claim into a patent-eligible application. *Alice*, 134 S. Ct. at 2355. In particular, based on the fact-finding and reasons provided by the Examiner at pages 8–9 of the Answer and pages 3–4 of the Final Office Action, we concur with the Examiner's determination that the additional elements or combination of elements recited in the claim amount to no more than mere instructions to implement the idea on a computer using generic computer equipment to perform generic computer functions that are well-understood, routine, and conventional activities previously known to the pertinent industry. *See Alice*, 134 S. Ct. 2357 (finding "conventional steps" insufficient to supply an "inventive concept").

As the Examiner finds (Ans. 8; Final Act. 3–4), claim 1 is directed to and the Specification discloses conventional computer activity and equipment for performing the steps of the method. *See* Fig. 5 (depicting "Computer system 502"), Spec. ¶ 70 (disclosing a general purpose "computer or a computer system . . . that can perform computations" comprising "processor 504, memory 506, and storage 508"), ¶ 71 (disclosing that "Application 516 can include instructions that when executed by computer 502 cause computer 502 to perform one or more processes that are implicitly or explicitly described in this disclosure").

Appellant's arguments do not reveal reversible error in the Examiner's analysis and factual findings in this regard.

Appellant's contentions that the "claims improve another technology, namely, the technology of circuit design and manufacturing" (Appeal Br. 17) and the method "results in an improved numerical synthesis process that uses an improved way for discretizing cell sizes" (Reply Br. 9) are not persuasive because they are conclusory and Appellant does not provide an adequate technical explanation to support them. Attorney argument is not evidence. *In re De Blauwe*, 736 F.2d 699, 705 (Fed. Cir. 1984).

Moreover, the mere fact that the claim seeks to limit the use of the abstract idea "'to a particular technological environment,'" i.e., the technology of circuit design and manufacturing, without more, does not transform the abstract idea into a patent-eligible invention. *Alice*, 134 S. Ct. at 2358 (quoting *Bilski v. Kappos*, 561 U.S. 593, 610–11 (2010)).

Appellant's contention that the Examiner "fails to properly state a § 101 rejection in accordance with the instructions that were specified in the July 2015 Update" (Appeal Br. 13–14) is not persuasive of reversible error in the Examiner's rejection because determining whether a claim is directed to an abstract idea under § 101 is not limited to the guidance provided in the July 2015 Update. Rather, as noted above and as we apply here, it is the two-step framework from *Alice* that is used for making such determination.

Appellant's argument that the claims are not directed to any of the four categories of abstract ideas provided in the July 2015 Update (Appeal Br. 16) is misplaced because, as previously discussed above, the Examiner properly determines that the claims are directed to the abstract idea of mathematical relationship/algorithms, which corresponds to category (4) of the July 2015 Update, i.e., "a mathematical algorithm, relationship, formula, or calculation."

We do not find Appellant's contentions at pages 14–15 of the Appeal Brief regarding the Examiner oversimplifying the claimed subject matter and that the claims are not directed to an abstract idea based on *Alice* persuasive of reversible error in the Examiner's rejection because they are conclusory and Appellant does not provide an adequate explanation to support them. *De Blauwe*, 736 F.2d at 705.

We, therefore, determine that claim 1 is directed to an abstract idea and fails to recite an inventive concept sufficient to transform the abstract idea into patent-eligible subject matter.

Although claims 7 and 17 are directed to an "apparatus" (claim 7) and a "non-transitory computer-readable storage medium" (claim 17), respectively, each of these claims recites limitations nearly identical to claim 1. *Compare* claim 1 (Appeal Br. 23), *with* claim 7 (Appeal Br. 24–25) and claim 17 (Appeal Br. 26–27).

Thus, for principally the same reasons discussed above with respect to claim 1, we determine that claims 7 and 17 are likewise directed to the abstract idea of a mathematical algorithm and do not contain an inventive concept sufficient to transform the nature of the claims into a patent-eligible application.

Accordingly, we affirm the Examiner's rejection of claims 1–12 and 17–22 under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

Rejection 2

Appellant argues claims 1–12 and 17–22 as a group. Appeal Br. 17. We select claim 1 as representative and the remaining claims subject to this rejection stand or fall with claim 1. 37 C.F.R. § 41.37(c)(1)(iv).

The Examiner determines that the combination of Morgenshtein and Scott suggests a method satisfying all of the steps of claim 1 and thus, concludes that the combination would have rendered the claim obvious. Final Act. 4–7; *see also* Ans. 9–15.

Appellant argues that the Examiner's rejection of claim 1 should be reversed because the cited references do not teach or suggest the "computing a delay from an input of the driver cell to an output of the optimizable cell" and "wherein instantiating the second library cell at the optimizable cell would improve the delay from the input of the driver cell to the output of the optimizable cell" recitations of the claim. Appeal Br. 19–21.

In particular, Appellant contends that the "term 'delay' in Scott merely refers to the delay through a single cell . . . and does not refer to the delay from an input of the driver cell to the output of the optimizable cell." *Id.* at 20. Appellant further contends that "cut 98" in Figure 5 of Scott does not correspond to a circuit path from an input of the driver cell to an output of the optimizable cell and that "Morgenshtein does not cure the above-mentioned deficiencies in Scott." *Id.* at 21.

We do not find Appellant's arguments persuasive based on the fact-finding and reasoning provided by the Examiner at pages 4–7 of the Final Office Action and pages 9–15 of the Answering Brief.

On the record before us, we find that a preponderance of the evidence and sound technical reasoning support the Examiner's analysis and

determination that the combination of Morgenshtein and Scott suggests a method satisfying all of the steps of claim 1, and the Examiner's conclusion that the combination would have rendered the claim obvious. Morgenshtein ¶¶ 32–34, 137–143, 151, 206, Fig. 2; Scott ¶¶ 5–7, 15, 16, 116–118, 124, Fig. 5.

As the Examiner finds (Final Act. 6), Scott teaches "performing a timing analysis" on the selected gate sizes from the available library of gate sizes (Scott ¶¶ 116–117), which corresponds to the "computing a delay from an input of the driver cell to an output of the optimizable cell" recitation of claim 1.

As the Examiner further finds (Final Act. 6; Ans. 12–13), Scott also suggests the "wherein instantiating the second library cell at the optimizable cell would improve the delay from the input of the driver cell to the output of the optimizable cell" recitation of the claim. In particular, we concur with the Examiner's analysis and findings that paragraph 7 of Scott suggests that by decreasing the size of a gate, the input capacitance is decreased, which allows for faster switching and a decreased (smaller) delay and that paragraph 118 of the reference suggests that selecting new gates sizes would be performed to minimize delays.

Appellant's contentions that the term "delay" in Scott merely refers to the delay through a single cell and does not refer to the delay from an input of the driver cell to the output of the optimizable cell (Appeal Br. 20) and regarding "cut 98" of Figure 5 of Scott (*id.* at 21) are not persuasive of reversible error because they are largely conclusory and Appellant does not adequately explain them. *De Blauwe*, 736 F.2d at 705.

Appellant argues that the Examiner's findings and analysis regarding "Equation (4)" of the Specification (Spec. ¶ 58) for computing delay at pages 9–14 of the Answer are "incorrect" because the input capacitance and delay terms of the equation are inversely proportional. Reply Br. 9–11. In particular, Appellant contends that "simply decreasing the input capacitance of an optimizable cell does not decrease the delay from the input of the driver cell to the output of the optimizable cell." *Id.* at 11; *see also* Appeal Br. 19 (arguing that "decreasing C_1 does not necessarily decrease the delay D_1 because the delay equation has a term that is inversely proportional to C_1").

We do not find Appellant's arguments in this regard persuasive of reversible error based on the fact-finding and for the well-stated reasoning provided by the Examiner at pages 9–13 of the Answer and pages 6–7 of the Final Office Action. In particular, we agree with the Examiner's simplification of Equation 4 and finding that none of the terms in the equation are inversely proportional to the input capacitance and, therefore, decreasing the input capacitance would decrease the delay (Ans. 10–11).

As the Examiner finds (Ans. 11–12), paragraph 7 of the Scott reference also explicitly teaches that by decreasing the size of a gate, the input capacitance is decreased and allows for "faster switching," which corresponds to a decrease in the delay. *See* Scott ¶ 7 (disclosing that "decreasing the size of gate **12**$_2$ and gate **12**$_3$ decreases the size of their respective input capacitance, also allowing faster switching").

Appellant's argument, without more, does not reveal reversible error in the Examiner's analysis and factual findings in this regard.

Accordingly, we affirm the Examiner's rejection of claims 1–12 and 17–22 under 35 U.S.C. § 103 as obvious over the combination of Morgenshtein and Scott.

DECISION/ORDER

The Examiner's rejections of claims 1–12 and 17–22 are affirmed.

It is ordered that the Examiner's decision is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED