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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte PAR S. WESTLUND and LARS-OLOF B. SVENSSON

Appeal 2017-004298
Application 14/510,946
Technology Center 2100

Before JOHN A. JEFFERY, THU A. DANG, and ALEX S. YAP, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's decision to reject claims 1–20. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

STATEMENT OF THE CASE

Appellants' invention is a memory system for multiple clients where every client is connected to (1) an operation bus to pass instructions; (2) a key bus to pass search keys to the memory system; and (3) a priority bus to pass results to the clients. The system uses plural hash content addressable blocks, where each block comprises bus select logic, key memory, select logic, and output logic. *See generally* Abstract; Spec. ¶¶ 9–27; Figs. 1–3. Claims 1 and 10 are illustrative:

1. A memory system comprising:

an interface to a plurality of clients, the interface comprising:

a plurality of operation buses used to pass instructions from the clients to the memory system, wherein every client in the plurality of clients is connected to one operation bus in the plurality of operation buses,

a plurality of key buses used to pass search keys from the clients to the memory system, wherein every client in the plurality of clients is connected to one key bus in the plurality of key buses, and

a plurality of priority buses used to pass results from the memory system to the clients, wherein every client in the plurality of clients is connected to one priority bus in the plurality of priority buses; and

a plurality of hash content addressable blocks, each hash content addressable block in the plurality of hash content addressable blocks comprising:

bus select logic connected to at least one operation bus in the plurality of operation buses and at least one key bus in the plurality of key buses, the bus select logic being configured to operate on data from a selected operation bus and a selected key bus for a selected client from a plurality of clients,

key memory that stores a plurality of output indices,

select logic that selects an output index from the plurality of output indices based on key data received from the selected key bus and based on operation data received from the selected operation bus, and

output logic connected to the plurality of priority buses, wherein the output logic outputs the output index to a priority bus for the selected client.

10. A memory system hash content addressable block comprising:

bus select logic connected to a plurality of client buses, each client bus including a key bus section and an operation bus

section, the bus select logic being configured to operate on data from a selected client bus from the plurality of client buses;

key memory that stores a plurality of output indices, each output index in the plurality of output indices being stored with an associated key;

select logic that based on a search key received from the key bus section for the selected client bus generates a key memory index and uses the key memory index to access from the key memory an output index from the plurality of output indices;

output logic connected to a plurality of priority buses, each of the priority buses being associated with a client bus from the plurality of client buses;

wherein the output logic outputs the output index to a priority bus associated with the selected client bus.

THE REJECTIONS

The Examiner rejected claims 10–15 under 35 U.S.C. § 112(b) as indefinite. Final Act. 2.[1]

The Examiner rejected claims 1–6, 8–13, and 15–20 under 35 U.S.C. § 103(a) as unpatentable over Choubal (US 2006/0018330 A1; Jan. 26, 2006), Melchior (US 6,226,710 B1; May 1, 2001), and Becca (US 2004/0001380 A1; Jan. 1, 2004). Final Act. 3–19.

The Examiner rejected claims 7 and 14 under 35 U.S.C. § 103(a) as unpatentable over Choubal, Melchior, Becca, and Patra (US 6,725,326 B1; Apr. 20, 2004). Final Act. 19–20.

[1] Throughout this opinion, we refer to (1) the Final Rejection mailed June 17, 2016 ("Final Act."); (2) the Appeal Brief filed September 27, 2016 (supplemented October 14, 2016) ("App. Br."); (3) the Examiner's Answer mailed December 9, 2016 ("Ans."); and (4) the Reply Brief filed January 17, 2017 ("Reply Br.").

THE INDEFINITENESS REJECTION

The Examiner finds that independent claim 10 is indefinite because it is unclear whether the recited "memory system hash content addressable block" refers to a memory system or a hash content addressable block. Final Act. 2.

Appellants argue that because the last noun, "block," is preceded by other nouns that are used adjectively to modify the last noun, the term is clear under common grammatical rules. App. Br. 11–12; Reply Br. 1–2.

ISSUE

Has the Examiner erred in rejecting claim 10 under § 112(b) by finding that the preamble can be interpreted as either a "memory system" or a "hash content addressable block"?

ANALYSIS

As noted above, the key term in this dispute is the "memory system hash content addressable block" in claim 10's preamble. Although this term is somewhat unusual, that does not mean it is indefinite particularly where, as here, the term's meaning can be reasonably ascertained from the claim itself.

Despite the Examiner's findings to the contrary, skilled artisans would understand that a "memory system hash content addressable *block*" is a block whose characteristics are indicated by its preceding modifying terms, such that the block not only pertains to a "memory system," but is also hash-content addressable. *Accord* App. Br. 11 (noting that the term "memory

system hash content addressable block" is synonymous with "hash content addressable block for a memory system").

To construe the preamble as directed to a memory system—not a block—as the Examiner proposes (Final Act. 2; Ans. 6) ignores the preamble's remaining terms, namely "hash content addressable block," thus rendering them meaningless. No reasonable interpretation of claim 10 justifies such a construction, for it is well settled that *all* recited terms must be considered when construing claims. *See In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970); *see also Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) ("[C]laims are interpreted with an eye toward giving effect to *all* terms in the claim.") (emphasis added).

This is not a case where claim 10's preamble is amenable to two or more plausible constructions (e.g., a memory system or a block) to render the claim indefinite. *See Ex parte Miyazaki*, 89 USPQ2d 1207, 1211 (BPAI 2008) (precedential). Rather, this is a case where there is only one reasonable interpretation—a block.

Therefore, we are persuaded that the Examiner erred in rejecting (1) independent claim 10 as indefinite, and (2) dependent claims 11–14 for similar reasons.

THE REJECTION OVER CHOUBAL, MELCHIOR, AND BECCA

The Examiner finds that Choubal, Melchior, and Becca teach or suggest the memory system of claim 1, and, based on these collective teachings, concludes that the claim would have been obvious. Final Act. 3–8.

Appellants argue that the Examiner's reliance on Choubal is misplaced because (1) Choubal's single external memory is not content addressable, nor does it include key memory and output logic, and (2) the single bidirectional bus renders bus select logic unnecessary. App. Br. 18–19; Reply Br. 6–7. Appellants add that not only is there no plausible way to combine the cited references to produce the claimed invention, the Examiner failed to show a proper motivation to combine the references not only in the rejection of claim 1, but also for claims 2 to 19. App. Br. 20–26; Reply Br. 7–10.

ISSUES

I. Under § 103, has the Examiner erred in rejecting claim 1 by finding that Choubal, Melchior, and Becca collectively would have taught or suggested plural hash content addressable blocks, each block comprising the recited bus select logic, key memory, select logic, and output logic?

II. Is the Examiner's proposed combination of the cited references supported by articulated reasoning with some rational underpinning to justify the Examiner's obviousness conclusion?

ANALYSIS

Claims 1, 10, and 16

We begin by noting that the format of the Examiner's rejection of claim 1 is somewhat unusual because it does not follow the typical format of (1) articulating findings from one primary prior art reference with respect to the recited limitations; (2) identifying particular deficiencies in the primary reference with respect to the recited limitations; (3) citing teachings from

one or more other prior art references to cure those acknowledged deficiencies; and (4) explaining why ordinarily skilled artisans would have combined the teachings of secondary references with those of the primary reference to render the claim obvious. *Accord* App. Br. 20–21 (noting that the Examiner's rejection of claim 1 runs counter to the typical methodology used to show obviousness).

Nevertheless, on this record, we see no harmful error in the Examiner's rejection despite its somewhat unorthodox approach. It is well settled that to establish a factual basis to support the legal conclusion of obviousness, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966) (noting that 35 U.S.C. § 103 leads to three basic factual inquiries: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the art). Furthermore, the Examiner's obviousness rejection must be based on

> "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" . . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Although the Examiner must determine the scope and content of the prior art in obviousness rejections, the Examiner's designated order of prior art references is of no consequence. *See In re Mouttet*, 686 F.3d 1322, 1333 (Fed. Cir. 2012) ("[W]here the relevant factual inquiries underlying an

obviousness determination are otherwise clear, characterization by the examiner of prior art as 'primary' and 'secondary' is merely a matter of presentation with no legal significance."). Rather, what matters is whether the Examiner clearly articulated the relevant factual inquiries based on those references in reaching an obviousness conclusion that is supported by some articulated reasoning with rational underpinning. *See id.*; *see also KSR*, 550 U.S. at 418. Therefore, despite Appellants' arguments regarding the propriety of citing Choubal as a primary reference in the rejection (App. Br. 20), such arguments regarding the order of the references are not persuasive given the cited references' collective teachings.

Turning to the rejection when considered in light of the Examiner's further explanation in the Answer, the Examiner's findings and conclusions in the rejection—including those regarding the disputed hash content addressable block limitation—are not based on any single reference alone, but rather the collective teachings of the three cited references. *See* Final Act. 3–8; Ans. 11–16.

Claim 1 recites, in pertinent part, plural hash content addressable blocks, where each block comprises the recited bus select logic, key memory, select logic, and output logic. On page 11 of the Answer, the Examiner explains that Choubal's Figure 6 shows multiple bus connections to a memory controller 206 comprising caches that are said to contain memory portions or "blocks." Although the Examiner acknowledges that these "blocks" are not *hash content addressable*, the Examiner nevertheless cites Melchior for teaching that content addressable memory is known in the art, and that the recited hash content addressable blocks would have been obvious over the cited references' collective teachings. *See* Ans. 12 (citing

Final Act. 5). Appellants' arguments regarding Choubal's individual shortcomings in this regard (App. Br. 19; Reply Br. 6–7), do not show nonobviousness because the rejection is based on the cited references' collective teachings. *See In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

Appellants' arguments regarding Choubal's alleged deficiencies regarding the recited bus select logic (App. Br. 19) are likewise unavailing. As the Examiner explains, Choubal's memory controller 10 in Figure 1 selects a particular client according to a predefined scheme to access external memory 14. Final Act. 6 (citing Choubal ¶ 7). Choubal's Figures 5 and 6 provide similar functionality in this regard. *See* Choubal ¶¶ 37, 42–43. *Accord* App. Br. 18–19.

Even assuming, without deciding, that Choubal is limited to a single bidirectional bus 214 in Figure 6 thus precluding the need for bus select logic as Appellants contend, the Examiner's rejection is not based solely on Choubal in this regard, but also on Melchior. *See* Final Act. 6; Ans. 12–13. As shown in Melchior's Figure 1, content addressable memory (CAM) engine 100 is connected to command bus 120 and data bus 116 that the Examiner maps to the recited operation and key buses, respectively. Final Act. 3–4; Melchior, col. 8, ll. 27–42.

Considering Choubal and Melchior collectively, then, the combination predictably yields a hash content addressable block not only with bus select logic connected to at least one operation and key bus, but also the recited key memory and select logic as the Examiner indicates. Final Act. 6–7; Ans. 13. Such an enhancement uses prior art elements predictably according to their established functions—an obvious improvement. *See KSR*, 550 U.S.

at 417. *See also* Ans. 15–16 (explaining why ordinarily skilled artisans would have combined Melchior with Choubal).

We reach a similar conclusion regarding the Examiner's reliance on Becca in connection with the recited output logic limitation. Final Act. 7–8; Ans. 13, 15–16. Here again, the Examiner's proposed combination uses prior art elements predictably according to their established functions. *See KSR*, 550 U.S. at 417. Moreover, Appellants' arguments regarding Choubal's individual shortcomings in this regard (App. Br. 19) do not show nonobviousness where, as here, the rejection is based on the cited references' collective teachings. *See Merck*, 800 F.2d at 1097.

Appellants' contention that there is no plausible way to combine the cited references (App. Br. 21–22) is unavailing. It is well settled that "a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *Mouttet*, 686 F.3d at 1332 (citations omitted). Nor is the test for obviousness whether a secondary reference's features can be bodily incorporated into the structure of the primary reference. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). "Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *Id.* And here, the Examiner's proposed combination reasonably satisfies that test, for the proposed combination predictably uses prior art elements according to their established functions to yield a predictable result. *See KSR*, 550 U.S. at 417.

Although the Choubal/Melchior/Becca system would arguably yield *one* hash content addressable block with the four recited elements, namely bus select logic, key memory, select logic, and output logic, we see no error in the Examiner's conclusion at least to the extent that providing *plural* hash

content addressable blocks in lieu of a single block would have been at least an obvious variation. *See* Final Act. 4–5; Ans. 10–11 (finding no patentable distinction in the claimed invention's duplicated buses and blocks). And to the extent that Appellants contend that the Examiner's proposed combination would somehow render the cited prior art unsuitable for its intended purpose (*see* App. Br. 21–22), there is no persuasive evidence on this record to substantiate such a theory.

On this record, then, the Examiner's proposed combination of the cited references is supported by articulated reasoning with some rational underpinning to justify the Examiner's obviousness conclusion. We reach this conclusion not only for the independent claims, but also the dependent claims as well. Although Appellants argue that the Examiner did not discuss the motivation to combine the references for claims 2 to 19 (App. Br. 26), the Examiner's rejection of independent claims 10 and 16 and dependent claims 2–6, 8, 9, 11–13, 15, and 17–20[2] is based on the same references cited in connection with claim 1, and the Examiner's articulated reason to combine those references likewise applies to those claims despite the references teaching or suggesting additional recited features. In short, these additional features use prior art elements predictably according to their established functions—an obvious improvement. *See KSR*, 550 U.S. at 417.

[2] Although Appellants omit claim 20 from the combinability argument regarding claims 2 to 19 (App. Br. 26), we nonetheless address claim 20 here as well. Moreover, because claims 7 and 14 were rejected separately over Choubal, Melchior, Becca, and Patra (Final Act. 19–20), we find sufficient reason to combine the cited references for the reasons noted above and by the Examiner. *See id.*

Therefore, we are not persuaded that the Examiner erred in rejecting claim 1, and claims 10 and 16 not argued separately with particularity.[3]

THE OTHER OBVIOUSNESS REJECTION

We also sustain the Examiner's obviousness rejections of claims 7 and 14. Final Act. 19–20. Because these rejections are not argued separately with particularity,[4] we are not persuaded of error in these rejections for the reasons previously discussed.

CONCLUSION

The Examiner erred in rejecting claims 10–15 under § 112(b), but did not err in rejecting claims 1–20 under § 103.

DECISION

We affirm the Examiner's decision to reject claims 1–20.

Because the rejection of each appealed claim is affirmed on at least one of the grounds specified in the Office Action from which the appeal was taken, the Examiner's decision to reject claims 1–20 is affirmed. *See* 37 C.F.R. § 41.50(a)(1).

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[3] Although Appellants nominally argue the Examiner's rejection of claims 10 and 16 separately (*see* App. Br. 26–36), Appellants reiterate arguments similar to those for claim 1 which we find to be unpersuasive for the reasons previously discussed. Accordingly, we group these claims together.

[4] Claims 7 and 14 are included in the range of claims listed in connection with Appellants' combinability arguments for claims 2 to 19, and we find sufficient reason to combine the cited references for the reasons noted above and by the Examiner. *See* Final Act. 19–20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED