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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/746,719	09/09/2010	Schumann Rafizadeh	20788.0001USWO	1806

52835 7590 11/26/2018
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EXAMINER

SCHNEE, HAL W

ART UNIT	PAPER NUMBER
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2132

NOTIFICATION DATE	DELIVERY MODE
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11/26/2018

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte SCHUMANN RAFIZADEH, PAUL WILLMANN,
YIJI LIN, and YING HU

Appeal 2017-003270
Application 12/746,719¹
Technology Center 2100

Before JOHN P. PINKERTON, JON M. JURGOVAN, and
NABEEL U. KHAN, *Administrative Patent Judges*.

PINKERTON, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1–4, 6, 7, 9, and 12–14, which constitute all of the claims pending in this application. Claims 5, 8, 10, and 11 are canceled. We have jurisdiction under 35 U.S.C. § 6(b).²

We affirm.

¹ Appellants identify Suzhou One World Technology Co., Ltd. as the real party in interest. App. Br. 6.

² An oral hearing was held in this case on November 7, 2018.

STATEMENT OF THE CASE

Introduction

Appellants generally describe the disclosed and claimed invention as related to a flash-based storage device, and more particularly to utilizing flash-based storage modules in an array format. Spec. ¶ 1.³

Claim 1 is representative and reproduced below (with the disputed limitations italicized):

1. A flash module array system comprising:

an enclosure including:

one or more physical input/output (I/O) interfaces communicable with a device external to the enclosure and configured to receive read and/or write commands from the device;

a plurality of flash module arrays, each including multiple flash memory modules; and

a flash module array controller directly communicable with the one or more physical I/O interfaces and the plurality of flash module arrays, the flash module array controller including:

a block mapping unit, configured to map addresses to a plurality of data blocks of the multiple flash memory modules and convert a logical address received by the one or

³ Our Decision refers to the Final Office Action mailed Apr. 18, 2016 (“Final Act.”); Appellants’ Appeal Brief filed Aug. 29, 2016 (“App. Br.”) and Reply Brief filed Dec. 20, 2016 (“Reply Br.”); the Examiner’s Answer mailed Oct. 20, 2016 (“Ans.”); and the Specification filed Nov. 30, 2012 (“Spec.”).

more physical I/O interfaces from the device external to the enclosure to a physical address of the multiple flash memory modules, and to convert the physical address of the multiple flash memory modules, to the logical address for the device external to the enclosure, wherein a host-based mapping unit is not utilized and there is *more than one flash module array for each block mapping unit*.

App. Br. 35 (Claims App'x).

Rejections on Appeal

Claims 1–4, 6, 7, 9, and 12–14 stand rejected under 35 U.S.C. § 112, first paragraph, for failing to comply with the written-description requirement. Final Act. 6–7.

Claims 1–4, 6, 7, 9, and 12–14 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventors regard as the invention. Final Act. 7–8.

Claims 1–4, 9, 12, and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitahara (US 2008/0098158 A1; published Apr. 24, 2008) and Whitt et al. (US 2006/0143506 A1; published June 29, 2006) (“Whitt”). Final Act. 8–14.

Claims 2, 6, and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitahara, Whitt, and Gonzalez et al. (US 2005/0144361 A1; published June 30, 2005) (“Gonzalez”). Final Act. 14–15.

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitahara, Whitt, and Wilson (US 2006/0173969 A1; published Aug. 3, 2006). Final Act. 15–16.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitahara, Whitt, and Bronson et al. (US 2003/0188074 A1; published Oct. 2, 2003) (“Bronson”). Final Act. 16–17.

ANALYSIS

Rejection of Claims 1–4, 6, 7, 9, and 12–14 Under § 112, First Paragraph

In the Final Office Action, the Examiner rejects independent claims 1 and 14 under 35 U.S.C. ¶ 112, first paragraph, as failing to comply with the written description requirement, and rejects claims 2–4, 6, 7, 9, 12, and 13 as being dependent on a rejected base claim. Final Act. 6–7.

The Examiner notes that independent claim 1 recites “a plurality of flash memory arrays” and that independent claim 14 recites “one or more flash module arrays.” *Id.* at 7. The Examiner also notes that both claims 1 and 14 recite “there is more than one flash module array for each block mapping unit,” and this implies “a plurality of block mapping units, with a plurality of arrays of flash memory modules for each block mapping unit.” *Id.* The Examiner finds, however, that the original disclosure includes “only a single block mapping unit 120 and a single flash module array 14, with the flash module array comprising multiple flash memory modules 141, 142 . . . 14N.” *Id.* (citing Fig. 1, ¶ 21 of published application US 2010/0325348 (the “348 publication”)). The Examiner further finds that

[n]owhere is there a description or suggestion of multiple block mapping units; nor is there a description or suggestion of multiple arrays of flash memory modules; nor is there a description or suggestion of multiple arrays of flash memory modules for the block mapping unit. These elements of claims 1 and 14 therefore constitute new matter.

Id.

Appellants argue that the disclosure in the Specification of “a flash [module] array” can be plural because “[f]lash module array is a collective noun and therefore considered plural when the group it names is considered to be made up of individuals, because the members can act on their own.” App. Br. 27 (citing Spec. ¶¶ 15, 23; Ex. 7). In this regard, Appellants argue that “[t]he flash module array are ‘individuals’ because the flash module array can act separately.” *Id.* (citing Ex. 7). According to Appellants, the illustration of one component, i.e., array, does not foreclose more than one of that component, and one of skill in the art “would realize that more than one ‘flash module array’ would logically be present.” *Id.* at 28–29 (citing Spec. ¶ 23; Ex. 1, Decl. of Krueger at ¶ 6; Ex. 2, Decl. of Xiao at ¶ 5; Ex. 3, Decl. of Rafizadeh at ¶¶ 8 and 12). Appellants also argue that “[t]here is no evidence of intent on the part of the inventors to limit the invention to one flash module array” and that paragraph 23 of the Specification states “[t]he capacity of flash memory storage is increased by utilizing multiple parallel flash memory modules as a flash array.” *Id.* at 29.

The test for compliance with the written description requirement under 35 U.S.C. § 112, first paragraph, is “whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). “[T]he disclosure as originally filed does not have to provide *in haec verba* support for the claimed subject matter at issue.” *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323 (Fed. Cir. 2000). Nevertheless, the disclosure must “clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed.” *Ariad*, 598 F.3d at

1351 (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1562–63 (Fed. Cir. 1991)).

We are not persuaded by Appellants’ arguments that the Examiner erred in finding that Appellants’ Specification only supports a single array containing multiple flash modules and does not reasonably convey to persons of ordinary skill in the art the claimed “plurality of flash module arrays” and “more than one flash module array for each block mapping unit.”

First, regarding Appellants’ argument that “flash module array” is a collective noun and, therefore, is considered “plural,” we agree with the Examiner’s finding “that ‘flash module array’ can be considered a plural collective noun, but in a plural collective noun it is the individual entities [acting on their own] that are plural, not the collective [noun].” Ans. 3. Appellants’ Exhibit 7 concerns the subject of “Sentence Agreement” of collective nouns, i.e., the subject and the verb must agree in number. *See* Ex. 7 (PDF of <http://www.infoplease.com/cig/grammar-style/collective-nouns.html>, last visited June 27, 2016). As the Examiner notes, Exhibit 7 uses the example of “the cast of a play” in which the word “cast” is a collective noun. The exhibit states that, when the members of the cast are functioning as a single unit, the collective noun “cast” takes the singular verb, as in the sentence stating, “The play’s cast *is* rehearsing for today’s show.” On the other hand, the exhibit states that, when the members of the cast are functioning as individual people doing separate things, the collective noun “cast” takes the plural verb, as in the sentence stating, “The play’s cast *are* rehearsing their lines.” Thus, as the Examiner finds, although use of the “play’s cast” requires a plural verb when its members act individually, the

word “‘cast’ itself is not plural—there is only one cast in the play, not multiple casts.” Ans. 3. Similarly, as the Examiner finds, and we agree, “an array can be considered a plural collective noun that contains multiple flash modules. But this does not imply a plurality of arrays.” *Id.*

Second, Appellants’ argument that the illustration of one component, i.e., array, does not foreclose more than one of that component (*see* App. Br. 28–29) is not persuasive in view of the disclosure in Appellants’ Specification. As the Examiner finds, and Appellants do not dispute, Figure 1 (the only drawing in the application) shows, and the Specification describes, one flash array controller 12, containing one block mapping unit 120, that is coupled to a single flash module array 14 comprising multiple flash memory modules 141–14N. Final Ans. 7 (citing Fig. 1, ¶ 21 of the ’348 publication). The Examiner also finds, and we agree, that Appellants’ Specification “only describe[s] mapping to the modules of a single array” and “[t]here is no description” in Appellants’ disclosure “of how mapping would be performed if more than one array were coupled to the block mapping module.” Ans. 4 (citing ¶¶ 23–25 of ’348 publication). Accordingly, we also agree with the Examiner’s finding that “[w]ithout a description of how the block mapping module would distribute data across two or more flash module arrays, a person of ordinary skill in the art would not be able to make and use the appellants’ claimed invention.” Ans. 4. We further agree with the Examiner’s findings that, if the system includes multiple block mapping units, the “situation becomes even more problematic” because “one needs to know how the multiple block mapping units are connected to one another and how they interact.” *Id.* at 5. As the Examiner finds, and we agree, “[s]ince the appellants’ original disclosure

does not describe the details essential to the structure and operations of a system with multiple block mapping units and multiple flash module arrays, such a system is not enabled by the disclosure.” *Id.*

Third, we are not persuaded by Appellants’ argument that one of skill in the art “would realize that more than one ‘flash module array’ would logically be present.” App. Br. 28–29 (citing Spec. ¶ 23; Ex. 1, Decl. of Krueger at ¶ 6; Ex. 2, Decl. of Xiao at ¶ 5; Ex. 3, Decl. of Rafizadeh at ¶¶ 8 and 12). We have reviewed the portions of the declarations cited by Appellants and find no evidence to support Appellants’ conclusion. Regarding paragraph 23⁴ of the Specification, it states that “[t]he capacity of flash memory storage is increased by utilizing multiple parallel flash memory modules as a flash array.” The Examiner finds, and we agree, that “this sentence shows that the appellants have envisioned adding memory modules to the array, not adding entire arrays.” Ans. 6.

Fourth, we are not persuaded by Appellants’ argument that there is no evidence of intent by the inventors to limit the invention to one flash module array (*see* App. Br. 29) because, as the Examiner finds, and we agree, there is no disclosure or suggestion in Appellants’ Specification of “multiple arrays of flash memory modules” or “multiple arrays of flash memory modules for the block mapping unit.” Final Act. 7. Appellants cite paragraph 6 of the Specification in support of this argument, which states that “the Flash Modules Array (FA) invention” provides a leap forward in solid state storage technology “by providing a solution that allows varying [the] number of off-the-shelf flash modules to be configured as a flexible

⁴ The Examiner notes that paragraph 23 of the Specification corresponds to paragraph 26 of the ’348 publication.

configuration of high capacity flash solid state storage devices.” We determine that this paragraph of the Specification is not persuasive of Appellants’ argument of “no intent by the inventors” to limit the invention to one flash module array because paragraph 6 does not describe or suggest multiple flash module arrays, but describes the advantages of varying the number of modules that can be configured as a flash module array.

Thus, we find that the disclosure of Appellants’ Specification fails to reasonably or clearly convey to those of ordinary skill in the art, as of the filing date, that the inventor had possession of the claimed “plurality of flash module arrays” and “more than one flash module array for each block mapping unit.” *See Ariad*, 598 F.3d at 135. Accordingly, we sustain the rejection of claims 1 and 14, and dependent claims 2–4, 6, 7, 9, 12, and 13, under § 112, first paragraph.

*Rejection of Claims 1–4, 6, 7, 9, and 12–14
Under § 112, Second Paragraph*

The Examiner notes that claims 1 and 14 each recite “a block mapping unit.” Ans. 7 (citing claim 1, line 8; claim 14, line 9). The Examiner also notes that the last two lines of claims 1 and 14 recite “there is more than one flash module array for each block mapping unit,” and finds that the term “each” implies multiple block mapping units. Ans. 7. The Examiner finds that, reading the claims in view of the Specification, a person of ordinary skill in the art would understand “a block mapping unit” to mean “one block mapping unit” and, therefore, claims 1 and 14 are “indefinite because they are self-contradictory, first reciting a single block mapping unit and then implying the existence of multiple block mapping units.” *Id.* at 4, 7–8. Because the Examiner finds that the scope of the claims could not be

definitively determined, the Examiner chose to interpret the claims, in view of the original disclosure, “as having a single block mapping unit and a single array of flash memory modules, the array comprising a plurality of flash memory modules.” Final Act. 8; Ans. 8.

In the Appeal Brief, Appellants argue that “[a]s indicated by the affidavits submitted during prosecution, those of skill in the art understand what is claimed when the claim is read in light of the specification.” App. Br. 33 (citing Ex. 1, Decl. of Krueger at ¶ 6; Ex. 2, Decl. of Xiao at ¶ 5; Ex. 3, Decl. of Rafizadeh at ¶ 8). Appellants also argue that “those of skill in the art interpret ‘a’ as at least one.” App. Br. 33. In the Reply Brief, in response to the Examiner’s finding that a person of ordinary skill in the art would understand “a block mapping unit” to mean “one block mapping unit,” Appellants argue that “[b]ased on the argument above for array, a block mapping unit can be one or more block mapping units.” Reply Br. 16.

At the oral argument in this case on November 7, 2018, Appellants’ counsel was asked about the Examiner’s indefiniteness rejection in view of the claim recitation that “there is more than one flash module array for each block mapping unit.” In response, Appellants’ counsel stated that the clause “each block mapping unit” is more appropriately read as “the block mapping unit.”⁵

We are not persuaded by Appellants’ arguments in the Briefs that the Examiner erred. Instead, we agree with the Examiner that a person of

⁵ Transcript of oral hearing, p. 15. In the event of further prosecution of this application, Appellants will have the opportunity to amend the claims if they desire to do so. Because the claims have not been amended by replacing the word “each” with “the” in this clause, we cannot consider the claims in a revised or amended form as of this time.

ordinary skill in the art, reading the claims in view of the Specification, would understand “a block mapping unit” to mean “one block mapping unit.” Ans. 7–8. As discussed *supra*, Appellants’ disclosure shows and describes only one block mapping unit. *See* Final Act. 7 (citing ’348 publication Fig. 1, ¶ 21). Appellants’ reliance on the Krueger, Xiao, and Rafizadeh declarations is unconvincing because Appellants have not identified, nor have we located, any portions of the declarations directly addressing this issue, much less providing persuasive evidence supporting Appellants’ position. Thus, we also agree with the Examiner that the claims are self-contradictory because they recite “a single block mapping unit” and then imply multiple block mapping units by reciting “there is more than one flash module array for each block mapping unit.” Ans. 7–8.

Thus, we conclude that claims 1 and 14 are indefinite under ¶ 112, second paragraph, because they are unclear and ambiguous in regard to whether one or more than one block mapping unit is claimed. *See In re Packard*, 751 F.3d 1307, 1313 (Fed. Cir. 2014) (“[C]laims are required to be cast in clear—as opposed to ambiguous, vague, indefinite—terms.”). Accordingly, we sustain the Examiner’s rejection of claims 1 and 14, and claims 2–4, 6, 7, 9, 12, and 13, under § 112, second paragraph.

Rejections of Claims 1–4, 6, 7, 9, and 12–14 Under § 103(a)

For the reasons discussed above, the scope of claims 1–4, 6, 7, 9, and 12–14 is unclear. Consequently, we do not sustain the rejections of claims 1–4, 6, 7, 9, and 12–14 under 35 U.S.C. § 103(a) because to do so would require speculation as to the scope of the claims. *See In re Steele*, 305 F.2d 859, 862–63 (CCPA 1962) (holding that the Board erred in affirming a rejection of indefinite claims under 35 U.S.C. § 103(a) because the rejection

was based on speculative assumptions as to the meaning of the claims). It should be understood, however, that our decision in this regard is *pro forma* and based solely on the indefiniteness of the claimed subject matter, and does not reflect on the adequacy of the prior art evidence applied in support of the rejections.

DECISION

We affirm the Examiner's rejection of claims 1–4, 6, 7, 9, and 12–14 under 35 U.S.C. § 112, first paragraph.

We affirm the Examiner's rejection of claims 1–4, 6, 7, 9, and 12–14 under 35 U.S.C. § 112, second paragraph.

We reverse the Examiner's rejection of claims 1–4, 6, 7, 9, and 12–14 under 35 U.S.C. § 103(a).

AFFIRMED