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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DANIEL S. FISHER and DANIEL R. ZAHARRIS

Appeal 2017-001959
Application 13/744,519
Technology Center 2100

Before JENNIFER S. BISK, JEREMY J. CURCURI, and PHILLIP A. BENNETT, *Administrative Patent Judges*.

BISK, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

Appellants[2], listed above, seek our review under U.S.C. § 134(a) of the Examiner's rejection of claims 1–20. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

BACKGROUND

Appellants' invention relates to a hybrid hard disk drive having a flash storage processor. Spec. ¶ 1.

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[1] Throughout this Decision, we have considered the Specification, filed January 18, 2013 ("Spec."), the Final Office Action, mailed July 17, 2015 ("Final Act."), the Appeal Brief, filed May 10, 2016 ("Appeal Br."), the Examiner's Answer, mailed September 12, 2016 ("Ans").

[2] Appellants identify the real party in interest as Avago Technologies. Appeal Br. 2.

Claim 1, reproduced below with indentation added, is illustrative of the claimed subject matter:

> 1. An apparatus comprising:
>
> a flash storage processor connected to a flash storage component and to an integrated circuit chip, wherein the flash storage processor is implemented apart from the integrated circuit chip;
>
> wherein the integrated circuit chip is indirectly connected to a host device via the flash storage processor and includes:
>
> a read/write channel device configured to communicatively couple to a hard disk drive assembly;
>
> a hard disk drive controller operatively coupled to the read/write channel device, the hard disk drive controller configured to operate the read/write channel device to store and to retrieve data on the hard disk drive assembly; and
>
> wherein the flash storage processor is configured to receive a first command and a second command from the host device, wherein the first command is directed to the integrated circuit chip and the second command is directed to the flash storage processor, and wherein the flash storage processor furnishes the first command to the integrated circuit chip without executing the first command and executes the second command.

THE REJECTIONS

1. Claims 1, 4, 5, 8, 10, 11, 13, 15, 16, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as being obvious over LaPanse (US 2010/0153635 A1, published June 17, 2010) and Sutardja (US 9,009,393 B1, issued Apr. 14, 2015). Final Act. 6–20.

2. Claims 2, 9, and 18 stand rejected under 35 U.S.C. § 103(a) as being obvious over LaPanse, Sutardja, and Ong (US 8,630,056 B1, issued Jan. 14, 2014). *Id.* at 20–23.
3. Claims 3 and 12 stand rejected under 35 U.S.C. § 103(a) as being obvious over LaPanse, Sutardja, and Tan (US 2011/0219206 A1, published Sept. 8, 2011). *Id.* at 24–26.
4. Claims 6 and 17 stand rejected under 35 U.S.C. § 103(a) as being obvious over LaPanse, Sutardja, and Peterson (US 2011/0320690 A1, published Dec. 29, 2011). *Id.* at 27–28.
5. Claims 7 and 14 stand rejected under 35 U.S.C. § 103(a) as being obvious over LaPanse, Sutardja, and Boyle (US 8,639,872 B1, issued Jan. 28, 2014 (filed May 31, 2011)). *Id.* at 28–30.

ANALYSIS

We review the appealed rejections for error based upon the issues identified by Appellants, and in light of the arguments and evidence produced thereon. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential).

We have considered all of Appellants' arguments and any evidence presented. We highlight and address specific findings and arguments for emphasis in our analysis below.

Claims 1, 4, 8, 10, 11, 13, 16, 19, and 20

Appellants argue claims 1, 4, 8, 10, 11, 13, 16, 19, and 20 together as a group. *See* App. Br. 17–23. Therefore, consistent with the provisions of 37 C.F.R. § 41.37(c)(1)(iv), we limit our discussion to independent claim 1. Claims 4, 8, 10, 11, 13, 16, 19, and 20 stand or fall with claim 1.

> The Examiner finds Sutardja teaches the claimed
>
> flash storage processor . . . configured to receive a first command and a second command from the host device, wherein the first command is directed to the integrated circuit chip and the second command is directed to the flash storage processor, and wherein the flash storage processor furnishes the first command to the integrated circuit chip without executing the first command and executes the second command [(the "command limitation")].

Final Act. 8–9 (citing Sutardja ¶¶ 13, 24). Specifically, the Examiner explains that Sutardja describes a host that directs commands to a flash storage processor (the solid-state disk controller ("SSD")) directed either to the SSD or to an integrated circuit chip (HDD system on chip ("HDD SOC")). Ans. 34–39. According to the Examiner, commands directed to the HDD SOC are not executed by the SSD, but instead are translated into an HDD command and passed to the HDD SOC for execution. *Id.* at 36–37.

Appellants argue that Sutardja does not teach the command limitation because the commands directed to the HDD SOC are "not suitable for execution by the HDD SOC" until they are translated by the SSD. App. Br. 20. According to Appellants, the claims require the flash storage processor to furnish "***THE*** same first command to the integrated circuit chip" and "not an alternate command generated by executing the original command through a translation process." *Id.* at 20–21.

In response, the Examiner explains that the claim language does not require the first command to be passed on to the integrated circuit chip without any change or translation. Ans. 36–37. We agree with the Examiner that Appellants' arguments are not commensurate with the claim language. Claim 1 only requires the flash storage processor to "furnish[] the first command to the integrated circuit chip *without executing the first*

command." As noted by the Examiner, when translating and passing on the command directed to the HDD SOC, Sutardja's SDD does not execute the command. *Id.* at 36. Appellants do not point to, nor could we find, any language in the claims that limits the flash storage processor to merely passing through the first command without any other change.

Further, Appellants do not point to, nor could we find in the Specification, any definition of the term "command" that would limit it to any particular format. In fact, according to the Specification, the first command "represents an [instruction/command] for accessing the hard drive assembly." Spec ¶¶ 4, 12, 24–27. We conclude the broadest reasonable interpretation of "command" encompasses both the format originally sent from the host device and any format forwarded on to the integrated circuit chip as long as each of the formats represents the same instruction for accessing the hard drive assembly. Given this construction, we find Appellants' arguments do not show error in the Examiner's factual findings or the ultimate finding of obviousness of representative independent claim 1 over the combination of LaPanse and Sutardja.

For these reasons, we sustain the Examiner's rejection of claims 1, 4, 8, 10, 11, 13, 16, 19, and 20.

Claim 5

Claim 5 depends indirectly from claim 1 and recites "wherein the host device is configured to issue the first command directly after issuing the second command, *wherein the first command represents instructions for accessing the hard disk drive assembly* and the second command represents instructions for accessing the flash storage component." App. Br. 29 (Claims App'x) (emphasis added). The Examiner relies on LaPanse as

disclosing this limitation. Final Act. 17–18 (citing LaPanse, Fig. 2, ¶¶ 8, 13, 24). Specifically, the Examiner explains that "LaPanse discloses determination logic of whether to store data received from a host via commands (plural—i.e. first, second, etc.) received from the host bus interface (commands from the host) either at the disc drive storage (hard disk drive assembly) or solid-state memory (flash)."). Ans. 41.

Appellants argue that "[n]either LaPanse nor Sutardja discloses, teaches or suggests that the host deice issue a first command including instructions for accessing the hard disk drive assembly." App. Br. 21. Appellants, however, do not address LaPanse's discussion of determination logic. On the record before us, we find Appellants' arguments do not show error in the Examiner's factual findings and the conclusion of obviousness of claim 5 over the combination of LaPanse and Sutardja.

Claim 15

Independent claim 15 recites a method comprising similar limitations as independent claim 1. For example, similar to the command limitation of claim 1, claim 15 recites "receiving a command derived from a host device, at a flash storage processor" and "providing the command to an integrated circuit chip when the command represents an instruction to access the at least one hard disk drive assembly." The Examiner relies the same teachings of Sutardja for these limitations. Final Act. 14–16.

Appellants emphasize the phrases "receiving *a command*" and "providing *the command*" when arguing that "[s]imilar to claim 1, [in claim 15] the same command (i.e., the command) received by the flash storage processor is provided to the integrated circuit chip." App. Br. 22.

According to Appellants, claim 15 requires "a pass through approach to accessing information." *Id.* at 23.

We do not agree with Appellants that claim 15, as written, is so limited. Instead, as discussed above with respect to claim 1, we agree with the Examiner that the claim language does not require the command be passed on to the integrated circuit chip without any change or translation. Consequently, we find Appellants' arguments do not show error in the Examiner's factual findings or the ultimate conclusion of obviousness of claim 15 over the combination of LaPanse and Sutardja.

Claims 2, 3, 6, 7, 9, 12, 14, 17, and 18

The Examiner rejects claims 2, 3, 6, 7, 9, 12, 14, 17, and 18 over a combination of LaPanse, Sutardja, and either Ong, Tan, Peterson or Boyle. Final Act. 20–30. For each of these claims, Appellants rely on the same arguments made with respect to claim 1. App. Br. 21–23. These arguments however, are not persuasive for the reasons discussed above. Consequently, we find Appellants' arguments do not show error in the Examiner's factual findings and the conclusion of obviousness of claims 2, 3, 6, 7, 9, 12, 14, 17, and 18.

DECISION

We affirm the Examiner's decision to reject claims 1–20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED