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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte YUKIYASU NAKAO, MASAYUKI IMAIZUMI, SHUHEI NAKATA, and NARUHISA MIURA[1]

Appeal 2017-000556
Application 14/245,539
Technology Center 2800

Before BRADLEY W. BAUMEISTER, JOSEPH P. LENTIVECH, DAVID J. CUTITTA II, *Administrative Patent Judges*.

BAUMEISTER, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 2–8. App. Br. 5–11.[2] Claim 1 has been cancelled. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

Pursuant to our discretionary authority under 37 C.F.R. § 41.50(b), we enter two new grounds of rejection for claim 2 under 35 U.S.C. § 103(a).

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[1] Appellants list Mitsubishi Electric Corporation as the real party in interest. Appeal Brief filed March 8, 2016 ("App. Br.") 1.

[2] Rather than repeat the Examiner's positions and Appellants' arguments in their entirety, we refer to the above-mentioned Appeal Brief, as well as the following documents, for their respective details: the Final Action mailed October 8, 2015 ("Final Act."); the Examiner's Answer mailed August 18, 2016 ("Ans."); and the Reply Brief filed October 12, 2016 ("Reply Br.").

STATEMENT OF THE CASE

Appellants describe the present invention as follows:

> A [silicon carbide ("SiC")] semiconductor device capable of increasing a switching speed without destroying a gate insulating film. In addition, in a SiC-[metal-oxide-semiconductor field effect transistor (MOSFET)] including [a negative-impurity-doped] n-type semiconductor substrate formed of SiC, a [positive-impurity-doped] p-type semiconductor layer is entirely or partially provided on an upper surface of a p-type well layer that has a largest area of the transverse plane among a plurality of p-type well layers provided in an n-type drift layer and is arranged on an outermost periphery immediately below a gate electrode pad. It is preferable that a concentration of an impurity contained in the p-type semiconductor layer be larger than that of the p-type well layer.

Abstract.

Independent claim 2, reproduced below, illustrates the claimed invention:

> 2. A silicon carbide semiconductor device comprising:
>
> a silicon carbide semiconductor substrate;
>
> a drift layer of a first conductivity type on a main surface of said silicon carbide semiconductor substrate;
>
> a cell region in a part of an upper layer of said drift layer, the cell region including a plurality of MOSFET cells each functioning as a MOSFET;
>
> a well layer of a second conductivity type in another part of said upper layer of said drift layer;
>
> an insulating film over said well layer;
>
> a gate electrode over said cell region and said insulating film;
>
> an interlayer dielectric film over said gate electrode;

> a gate pad over said well layer and electrically connected to said gate electrode through a contact hole of said interlayer dielectric film; and
>
> a source electrode connected to said well layer;
>
> wherein said contact hole orthogonally projects onto said well layer, and
>
> said well layer has a region which has a higher impurity concentration than a portion of said well layer that is not in said region.

Claims 2–8 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Okabe et al. ("Okabe") (US 5,169,793; issued Dec. 8, 1992), Kelberlau et al. (US 2003/0214012 A1; published Nov. 20, 2003) ("Kelberlau"), and Suzuki et al. (US 2008/0224150 A1; published Sept. 18, 2008) ("Suzuki"). Final Act. 3–8.[3, 4]

We review the appealed rejections for error based upon the issues identified by Appellants, and in light of the arguments and evidence produced thereon. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential).

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[3] Appellants assert that the Examiner additionally relies on Blake et al., "IGBT or MOSFET: Choose Wisely," International Rectifier (available at https://www.infineon.com/dgdl/Infineon-IGBT_or_MOSFET_Choose_Wisely-ART -v01_00-EN.pdf?fileId=5546d462533600a40153574048b73edc). App. Br. 5. The Examiner does not cite this reference in the rejection, though. *See* Final Act. 2–8; Ans. 2–16. Accordingly, we do not consider this reference on appeal. *See In re Hoch*, 428 F.2d 1341, 1342 n.3 (CCPA 1970) ("Where a reference is relied on to support a rejection, whether or not in a 'minor capacity,' there would appear to be no excuse for not positively including that reference in the statement of the rejection").

[4] The Examiner withdrew a previously issued rejection of claim 4 under 35 U.S.C. § 112, ¶ 2. Final Act. 8.

FINDINGS AND CONTENTIONS

The Examiner finds that Okabe discloses every limitation of claim 2 with two exceptions. Final Act. 3–4. According to the Examiner, "Okabe does not teach that the semiconductor device is a silicon carbide device [or] that its cells are MOSFET cells." *Id.* at 4. The Examiner finds that Okabe instead discloses a plurality of insulated gate bipolar transistor (IGBT) cells. *Id.* at 3.

The Examiner relies on Kelberlau for teaching that an IGBT has a same structure as a MOSFET, with the exception that whereas Okabe's MOSFET has an n-type substrate subjacent to the n-type drift region, an IGBT has a p-type substrate, forming a p-n junction between the substrate and drift regions. *Id.* at 4. The Examiner determines that

> it would have been obvious . . . to modify [Okabe's] semiconductor device by creating its substrate with an n-type of conductivity, instead of a p-type, creating by that a MOSFET device with MOSFET cells, wherein it is desirable to have a MOSFET with a structure of the Okabe's IGBT, extending by that a field of application of the design of the Okabe[] transistor.

Id.

The Examiner additionally finds that the combination of Okabe and Kelberlau does not teach that such a semiconductor device may be constructed specifically out of silicon carbide ("SiC"). *Id.* The Examiner relies on Suzuki for teaching that cell-type MOSFET devices may be made specifically of SiC. *Id.* The Examiner concludes that it would have been obvious to build a MOSFET according to the combination of Okabe and Kelberlau specifically from a SiC material system instead of silicon. *Id.* at 4–5. According to the Examiner, substituting SiC for silicon was known to produce a device that has a higher breakdown voltage. *Id.* at 5.

The Examiner further explains in the Answer that the rejection is *not* based on a theory that an IGBT and a MOSFET are interchangeable. Ans. 6. According to the Examiner, "[t]he prior art recognizes that IGBTs and MOSFETs have different characteristics and different properties and, consequently, they are used in the art for different applications." Ans. 5. The Examiner also re-explains the relied-upon motivation to combine the references:

> Multiple [examples of] prior art, including Okabe, recognize that MOSFETs and IGBTs have some differences in their operations. These differences and the recognition of these differences provide a sufficient reason for creating a MOSFET based on the Okabe'[s] IGBT[] because such [a] MOSFET would possess at least an advantage of a higher operating speed. The Office Action mailed 10/08/15 (the Office Action, hereafter) states (on page 4) that a reason for creating a MOSFET based on the structure of Okabe'[s] IGBT was to extend "a field of application of the design of [Okabe's] transistor[."] A needed modification for creating a MOSFET from the already created structure of [Okabe's] IGBT is very easy to implement. But as a consequence of such modification, a field of semiconductor devices would have a new modification of a MOSFET[] structure, *which*, in addition to its higher operating speed than an IGBT has, *may have other advantages (which may be interesting to find out and investigate)*.

Ans. 4–5 (emphasis added).

The Examiner again states,

> one of ordinary skill in the art at the time of the invention could [have] create[d] a MOSFET based on a disclosed structure of an IGBT: *One of ordinary skill in the art at the time of the invention would [have] recognize[d] that a needed modification is easy to implement, but as a consequence of such modification*, a field of semiconductor devices would have a new modification of a

> MOSFET[] structure, which, in addition to its higher operating speed than that of an IGBT, *may have some other advantages*.

Id. at 6 (emphasis added). "[T]he motivation[] for combining [the] prior art used by the Office Action for creating a MOSFET based on [Okabe's] IGBT is to create a modified MOSFET structure that was not known in the art." *Id.* at 9.

Appellants argue that the Examiner has not set forth a sufficient factual basis to support a conclusion of obviousness. Reply Br. 3. According to Appellants, the Examiner's conclusion that modifying Okabe's IGBT to a make it a MOSFET "may have some other advantages" constitutes "a general assertion that there may exist other and undetermined advantages. Reply Br. 3 (citing Ans. 6). Appellants urge that such an assertion "is not a sufficient reason to modify the prior art to achieve the claimed invention." Reply Br. 3.

ANALYSIS

We understand the Examiner's rationale for combining the cited prior art to be based on the following premises: (1) heavily doping a p-type layer under an IGBT's gate pad electrode was known to have beneficial effects for the IGBT, such as faster turn-off time and increased breakdown voltage (Okabe, Abstract); and (2) power MOSFETS also were known (*see generally* Kelberlau). We further understand the Examiner's rationale for combining the references to be based on the theory that modifying the substrate conductivity of Okabe would produce a MOSFET having a heavily doped p-type layer below the gate bonding pad electrode, and providing such a doped layer in a MOSFET merely would entail applying a known technique (in an IGBT) to a known device (a MOSFET) ready for the

improvement to yield predictable results. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007); *see also* MPEP § 2143(D).

The Examiner's motivation also could be viewed as being based on the theory that known work (heavily doping a layer below a gate pad electrode) in one field of endeavour (IGBT design) may prompt variations of it for use in a different field (MOSFET design) based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art. *See KSR*, 550 U.S. at 417; *see also* MPEP § 2143(F).

We agree with the Examiner on the first two premises—the benefits of heavily doping a p-type layer under an IGBT's gate pad electrode were known, and power MOSFETS also were known. However, the Examiner has not provided sufficient evidence or technical rationale for concluding that one of ordinary skill reasonably would have expected the inclusion of the heavily doped layer below a power MOSFET's insulated gate pad electrode to provide benefits or improvements similar to those that occur in an IGBT. *See generally* Final Act. Speculation that including the heavily doped layer may offer advantages that "may be interesting to find out and investigate" (Ans. 5) does not constitute evidence that the variation would be predictable.

For the foregoing reasons, Appellants have persuaded us of error in the Examiner's obviousness rejection of independent claim 2. Accordingly, we do not sustain the Examiner's rejection of that claim, or of claims 3–8, which depend from claim 2.

NEW GROUNDS OF REJECTION

Matsuki, Kelberlau, and Suzuki

Pursuant to our discretionary authority under 37 C.F.R. § 41.50(b), we enter a new ground of rejection for claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Matsuki (US 6,930,355 B2; issued Aug. 16, 2005), Kelberlau, and Suzuki.[5]

Matsuki's Figure 6 embodiment, reproduced below, discloses every element of independent claim 2 except for teaching that the device may be constructed of a silicon carbide material system:

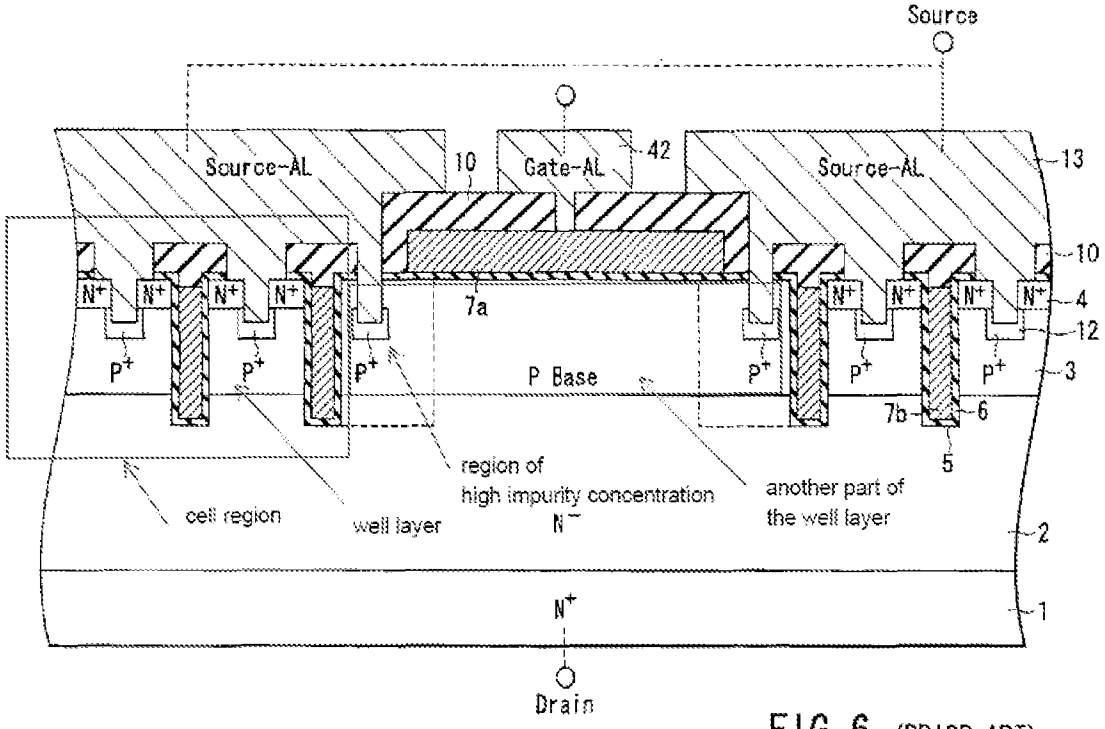

FIG. 6 (PRIOR ART)

[5] Kelberlau is relied upon only for providing evidence of the common meanings in the semiconductor arts of the terms "layer" and "well," as discussed *infra*.

Matsuki's Figure 6 more specifically depicts an N^+ semiconductor substrate 1 and an N^- drift layer 2 on a main surface of said semiconductor substrate. A cell region is located in a part of an upper layer of said drift layer, the cell region including a plurality of MOSFET cells each functioning as a MOSFET. *See* Matsuki, col. 1, ll. 22–26 (setting forth that the semiconductor devices are trench gate type power MOSFETs). The MOSFETs' trench gates extend through the P base 3 into the N^- drift layer 2. Matsuki, FIG. 6. As such, the recited "cell region" may be interpreted as reading on the regions of the P base 3 and portions of the upper layer of the N^- drift layer 2 in which the MOSFETs reside.

Matsuki's P base region 3 also reads on the claimed "well layer of a second conductivity type in another part of said upper layer of said drift layer." We note as a threshold matter that while Appellants may be their own lexicographers, Appellants do not expressly define the claim term "well layer." *See generally* Spec. Nor do Appellants point to any part of the record that would indicate the term "well layer" was commonly used in the semiconductor industry. *See generally* App. Br.; Reply Br.

We understand that within the context of semiconductor structures, the term "layer" more commonly referred to a region that covers substantially an entire surface of an underlying layer, such as a wafer-bonded layer, an epitaxially grown layer, or a layer that is diffused into substantially the entire surface of a pre-existing layer. *See, e.g.*, Matsuki, col. 3, ll. 35 (referring to "epitaxial *layer* 2" (emphasis added)). The term "well," in contrast, more commonly referred to a doped region that encompasses a relatively smaller surface portion of a larger, oppositely doped layer or substrate. *See, e.g.*, Kelberlau, ¶ 4; FIG. 1 (disclosing a high

resistivity *layer* 11 deposited on buffer layer 10B and disclosing p-*wells* 66 formed in the high resistivity *layer* 11). Because Appellants choose to conjoin these two terms, which traditionally connoted differing degrees of surface coverage, but Appellants do not provide any express definition for their terminology, we interpret Appellants' "well layer" to be broad enough to read on either a semiconductor "well" or a semiconductor "layer."

We further note that the claim language "a well layer of a second conductivity type in another part of said upper layer of said drift layer" only requires that the well layer be in *at least* a part of the upper layer of the drift layer other than the cell region. The claim language does not limit the well layer to being in *only* another part of the drift layer. As such, the claimed well layer reads on P base region 3 of Matsuki.

Figure 6 of Matsuki additionally discloses insulating oxide film 6 over the P base well region/layer 3. A gate electrode 7a/b is over said cell region and said insulating film. An interlayer dielectric film 10 is over the gate electrode. A gate pad 42 is over the well layer 3 and electrically connected to the gate electrode through a contact hole of the interlayer dielectric film. Source electrodes 13 are connected to the well layer 3.

A contact hole orthogonally projects through the interlayer dielectric film 10 for the gate pad 42 to electrically contact gate electrode 7a. These layers are over the well region/layer, so like Appellants' invention, the contact hole can be interpreted as orthogonally projecting *onto* the underlying well layer.

The well layer 3 also contains its own sub-region that has a higher impurity concentration than other portions of well region 3. Specifically, a P^+ contact region is disposed below the trench into which source electrode

13 is filled—the region that is adjacent the region under the gate electrode 7a.

We understand the drafters of the present claims to have been envisioning a structure wherein the higher impurity concentration region extends laterally, substantially coextensively with the length of gate electrode 7a. *See, e.g.*, Appellants' Figure 2, element 14 (depicting heavily doped junction termination extension region). However, claim 2 is written more broadly than this, such that the claimed higher impurity concentration region reads on the noted P+ contact region of Matsuki.

As noted above, Matsuki does not expressly disclose that the power MOSFET of Figure 6 may be composed of a silicon carbide material system. Suzuki, however, teaches that it was conventional to form vertical power MOSFET devices from silicon carbide. *See generally* Suzuki. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed Matsuki's MOSFET device from a silicon carbide material system in order to produce a device with a higher electric field breakdown strength than can be achieved with a silicon material system. Suzuki ¶ 6.

Takahashi, Matsuki, and Suzuki

Pursuant to our discretionary authority under 37 C.F.R. § 41.50(b), we enter a new ground of rejection for claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Takahashi (US 5,686,750; issued Nov. 11, 1997), Matsuki, and Suzuki.

Takahashi is directed to "[a] vertical field effect transistor [that] comprises a MOSFET cell zone which is formed in a principal surface of an N-type semiconductor substrate and in which a plurality of MOSFET cells

are formed and connected in parallel with one another." Takahashi, Abstract. Takahashi's embodiment that is primarily depicted in Figure 2C, in combination with the associated discussion, discloses every element of independent claim 2 with two exceptions. Takahashi does not disclose that its well layer has a region with higher impurity concentration, but Matsuki teaches this feature. Takahashi also does not disclose that the device may be constructed of a silicon carbide material system, but Suzuki teaches this feature. Motivation also exists for combining these two additional features.

More specifically, Takahashi discloses a semiconductor substrate 11. Takahashi FIG. 2C; col. 4, l. 21. Drift layer 12 of N^- conductivity type is disposed on a main surface of the substrate. *Id.* FIG. 2C. A region of MOSFET cells 6 is formed on the upper layer of the drift layer 12. *Id.* A P^- well layer 20 is formed in another part of the upper layer of the drift layer 12. *Id.* Gate oxide insulating film 13 is formed over said well layer 20, and a gate electrode 14 is formed over the insulating film 13. *Id.* An interlayer dielectric film 17 is formed over the gate electrode 14, and a gate finger 22 of a gate pad 4 is formed over the well layer 20 and electrically connect to the gate electrode through a contact hole of the interlayer dielectric film 17. *Id.* FIGs. 1A, 2C.

Field pate electrode 24 is connected to P^- well 20. *Id.* FIG. 2C. Takahashi discloses that the field plate electrode 24 of the peripheral zone is electrically connected to the source electrode 18 "so that the P-well of the peripheral zone is biased to the same potential as that of the source electrode." *Id.* col. 2, ll. 24–27. As such, it is reasonable to interpret Takahashi as disclosing that the source electrode is connected to the well layer, as claimed.

As noted above, Takahashi does not disclose the well layer 20 having a higher impurity concentration region. Matsuki teaches P+ impurity regions located in the P base layer 3, subjacent to the source electrode 13. Matsuki Fig. 6. It would have been obvious to one of ordinary skill in the art at the time of the invention to having included within Takahashi's Figure 2C embodiment, a heavily doped p^+ diffusion region within P^- well 20, below the field plate electrode 24, for making ohmic contact between the field plate / source electrode 24 and the P^- well 20, and thereby advantageously reducing resistance, as taught by Matsuki. *See* Matsuki, col. 4, ll. 42–47.

Regardless of whether the combination of Takahashi and Matsuki may teach or suggest using a silicon carbide material system, Suzuki, teaches that it was conventional to form vertical power MOSFET devices from silicon carbide. *See generally* Suzuki. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed a MOSFET device according to Takahashi and Matsuki specifically from a silicon carbide material system in order to produce a device with a higher electric field breakdown strength than can be achieved with a silicon material system. Suzuki ¶ 6.

CONCLUSIONS

We reverse the Examiner's obviousness rejection of claims 2–8 under 35 U.S.C. § 103(a).

Pursuant to our discretionary authority under 37 C.F.R. § 41.50(b), we enter a new ground of rejection for claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Matsuki, Kelberlau, and Suzuki.

Pursuant to our discretionary authority under 37 C.F.R. § 41.50(b), we enter a new ground of rejection for claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Takahashi, Matsuki, and Suzuki.

Although we decline to reject claims 3–8 pursuant to our discretionary authority under 37 C.F.R. § 41.50(b), we emphasize that our decision does not mean that the remaining claims are necessarily patentable. Rather, we merely leave the patentability determination of these claims to the Examiner. *See* MPEP § 1213.02.

DECISION

The Examiner's decision rejecting claims 2–8 is reversed.

Pursuant to our discretionary authority under 37 C.F.R. § 41.50(b), we enter two new grounds of rejection for claim 2 under 35 U.S.C. § 103(a).

Rule 41.50(b) provides that "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."
Rule 41.50(b) also provides the following:

> When the Board enters such a non-final decision, the appellant, within two months from the date of the decision, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:
>
> > (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new Evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the prosecution will be remanded to the examiner. The new ground of rejection is binding upon the examiner unless an amendment or new Evidence not previously of Record is made which, in the opinion of the examiner, overcomes the new ground of rejection

> designated in the decision. Should the examiner reject the claims, appellant may again appeal to the Board pursuant to this subpart.
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same Record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

Further guidance on responding to a new ground of rejection can be found in the Manual of Patent Examining Procedure (MPEP) § 1214.01 (9th Ed., Rev. 9, Nov. 2015).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED
37 C.F.R. § 41.50(b)