



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
13/849,427 03/22/2013 Yan Lin SNPS-2156US02 7109

36503 7590 09/27/2017
PVF -- SYNOPSIS, INC
c/o PARK, VAUGHAN, FLEMING & DOWLER LLP
2820 FIFTH STREET
DAVIS, CA 95618-7759

EXAMINER

AISAKA, BRYCE M

ART UNIT PAPER NUMBER

2851

NOTIFICATION DATE DELIVERY MODE

09/27/2017

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jeannie@parklegal.com
wendy@parklegal.com

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

*Ex parte* YAN LIN, YI-MIN JIANG,  
PHILLIP H. TAI, and LIN YUAN

---

Appeal 2016-008494  
Application 13/849,427  
Technology Center 2800

---

Before TERRY J. OWENS, CATHERINE Q. TIMM, and  
CHRISTOPHER C. KENNEDY, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

The Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1–18. We have jurisdiction under 35 U.S.C. § 6(b).

*The Invention*

The Appellants claim a method and non-transitory computer-readable instruction storage medium for pattern-based power-and-ground routing, and claim a method for creating vias during such routing. Claims 1 and 15 are illustrative:

1. In an electronic design automation (EDA) software tool, a method for pattern-based power-and-ground (PG) routing, the method comprising:

receiving a pattern for routing PG wires, wherein the pattern is described by a user using a pattern definition language, and wherein the pattern comprises a description of at least a shape, size, or relative location of one or more PG wires;

receiving an instantiation strategy for instantiating the pattern, wherein the instantiation strategy specifies an area of an integrated circuit (IC) design layout where PG wires based on the pattern are to be instantiated and specifies one or more net identifiers that are to be assigned to the instantiated PG wires; and

instantiating, by using a computer, the PG wires in the IC design layout based on the pattern and the instantiation strategy.

15. In an electronic design automation (EDA) software tool, a method for creating vias during pattern-based power-and-ground (PG) routing, the method comprising:

receiving a set of via rules, wherein each via rule specifies a type of via that is to be instantiated at an intersection between two PG wires that are in two different metal layers;

detecting an intersection between a first PG wire in a first metal layer and a second PG wire in a second metal layer;

selecting a via rule in the set of via rules based on a first pattern that was used to create the first PG wire and a second pattern that was used to create the second PG wire, wherein the first pattern and the second pattern are described by a user using a pattern definition language; and

instantiating, by computer, a via in the IC design layout at the intersection between the first PG wire and the second PG wire based on the selected via rule.

#### *The References*

Kiani	US 6,388,208 B1	May 14, 2002
Shibata	US 2005/0281119 A1	Dec. 22, 2005
Isomura	US 2010/0077373 A1	Mar. 25, 2010

#### *The Rejections*

The claims stand rejected as follows: claims 1–18 under 35 U.S.C. § 101 as claiming non-statutory subject matter, claims 1, 3, 4, 8,

10, 11, and 15 under 35 U.S.C. § 102(b) over Isomura, claims 2 and 9 under 35 U.S.C. § 103 over Isomura in view of Shibata, and claims 5–7, 12–14, and 16–18 under 35 U.S.C. § 103 over Isomura in view of Kiani.

#### OPINION

We affirm the rejections.

#### *Rejection under 35 U.S.C. § 101*

“Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.” 35 U.S.C. § 101. The Supreme Court stated in *Bilski v. Kappos*, 561 U.S. 593, 601 (2010) that “[t]he Court’s precedents provide three specific exceptions to § 101’s broad patent-eligibility principles: ‘laws of nature, physical phenomena, and abstract ideas.’” [*Diamond v.*] *Chakrabarty*, [447 U.S. 303,] 309, 100 S. Ct. 2204 [(1980)].” The Court further stated that limiting an abstract idea to a particular technological environment does not make the concept patentable. *See Bilski*, 561 U.S. at 610. Determining whether a claimed invention is patent-eligible subject matter requires determining whether the claim is directed toward a patent-ineligible concept and, if so, determining whether the claim’s elements, considered both individually and as an ordered combination, transform the nature of the claim into a patent-eligible application. *See Alice Corp. v. CLS Bank Int’l*, 134 S. Ct. 2347, 2350 (2014).

The Appellants’ claims 1 and 8 recite the patent-ineligible concept (abstract idea) of inputting into a software program a pattern definition language-defined PG wire routing pattern, inputting into the software program an instantiation strategy which specifies an IC design layout area

where PG wires based on the pattern are to be instantiated, and instantiating, using the software program, the PG wires, and IC design layout based on the pattern and the instantiation strategy. Claim 15 recites the patent-ineligible concept (abstract idea) of inputting into a software program a set of via rules, each of which specifies a type of via to be instantiated at an intersection between two wires in different metal layers, selecting from the set, using the software program, a rule based on a first pattern used to create a first PG wire in a first metal layer and a second pattern used to create a second PG wire in a second metal layer, both patterns being described by a user using a pattern definition language, and instantiating, using the software program, a via at the intersection between the first and second PG wires based upon the selected rule. Reciting in each claim that a computer instantiates the PG wires does not transform the nature of the claim into a patent-eligible application. *See Alice*, 134 S. Ct. at 2357–58 (“[S]imply implementing a mathematical principle on a physical machine, namely a computer, [i]s not a patentable application of that principle” (quoting *Mayo Collaborative Services v. Prometheus Labs.*, 566 U.S. 66, 84 (2012)) (citing *Gottschalk v. Benson*, 409 U.S. 63, 67 (1972))).

The Appellants assert that the Examiner failed to “provide a comparison between the subject matter of the claim that is being analyzed and concepts already found to be abstract in the body of case law” (Br. 15).

Patent-ineligible subject matter is not limited to subject matter which has been found to be patent ineligible in previous cases.

The Appellants assert that the claimed subject matter is not an uninstantiated concept (Br. 18–19).

Merely reciting that the PG wires are instantiated using a computer does not render the claimed subject matter patent eligible. *See Alice*, 134 S. Ct. at 2357–58.

Thus, we are not persuaded of reversible error in the rejection under 35 U.S.C. § 101.

*Rejections under 35 U.S.C. §§ 102(b) and 103*

The Appellants argue in two groups the claims rejected under 35 U.S.C. § 102(b): 1) claims 1, 8, 10, and 11, and 2) claims 3, 4, and 15 (Br. 19–23). We therefore limit our discussion to one claim in each of those groups, i.e., claims 1 and 15. Claims 8, 10, and 11 stand or fall with claim 1, and claims 3 and 4 stand or fall with claim 15. Although additional references are applied in the rejections of claims 2, 5–7, 9, 12–14, and 16–18 under 35 U.S.C. § 103, the Appellants do not provide a substantive argument as to the separate patentability of those claims (Br. 23–24). Consequently, claims 2 and 5–7 (which depend from claim 1) and claims 9 and 12–14 (which depend from claim 8) stand or fall with claim 1, and claims 16–18 (which depend from claim 15) stand or fall with claim 15. *See 37 C.F.R. § 41.37(c)(1)(iv) (2012)*.

“Anticipation requires that every limitation of the claim in issue be disclosed, either expressly or under principles of inherency, in a single prior art reference.” *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1255–56 (Fed. Cir. 1989).

Isomura applies “spacing rules between a wiring layer and a via layer to devices and wires for body bias power supply” (¶ 58) by searching and processing information from a wiring layer-via layer spacing rule table, a virtual figure table, a terminal figure table, an obstacle figure table, a net

table, a logic element table, a wire table, a via table, a wire protected area table, a terminal table, a layer table, a spacing table, a via type table and a via figure table, created from information registered in an arrangement/wiring database (¶¶ 64–107).

*Claim 1*

The Appellants assert that Isomura does not disclose a pattern described by a user using a pattern definition language (Br. 20).

The Examiner finds that “the routing of Isomura is carried out on a computer and must necessarily use a pattern definition language” (Ans. 6). The Appellants do not challenge that finding. Consequently, we accept it as fact. *See In re Kunzmann*, 326 F.2d 424, 425 n.3 (CCPA 1964).

The Appellants assert that Isomura does not disclose an instantiation strategy that specifies an area of an IC design layout where PG wires based on the pattern are to be instantiated or instantiate the PG wires in the IC design layout based on the pattern and the instantiation strategy (Br. 21).

The Examiner finds that Isomura determines a path that connects figures or routes all nets and specifies that wires may be placed in the pathway or the routing areas of the nets, and that this is an instantiation strategy (Ans. 7). The Appellants do not challenge that finding. Accordingly, we accept it as fact. *See Kunzmann*, 326 F.2d at 425 n.3.

*Claim 15*

The Appellants assert that Isomura does not select a via rule in a set of via rules based on a first pattern used to create a first PG wire and a second pattern used to create a second PG wire (Br. 23).

The Examiner finds that “a via type associates or selects a set of attributes corresponding to that via type with a particular via in the circuit

design, and must necessarily be chosen based on the circuit design or pattern elements which the via is connecting” (Ans. 8). The Appellants do not challenge that finding. Hence, we accept it as fact. *See Kunzmann*, 326 F.2d at 425 n.3.

For the above reasons we are not convinced of reversible error in the rejections under 35 U.S.C. §§ 102(b) and 103.

#### DECISION/ORDER

The rejections of claims 1–18 under 35 U.S.C. § 101 as claiming non-statutory subject matter, claims 1, 3, 4, 8, 10, 11 and 15 under 35 U.S.C. § 102(b) over Isomura, claims 2 and 9 under 35 U.S.C. § 103 over Isomura in view of Shibata and claims 5–7, 12–14, and 16–18 under 35 U.S.C. § 103 over Isomura in view of Kiani are affirmed.

It is ordered that the Examiner’s decision is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED