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NGUYEN, LINH M

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PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NETLIST, INC.
Requester,

v.

Patent of SMART MODULAR TECHNOLOGIES, INC.
Patent Owner

Appeal 2016-006595
Reexamination Control No. 95/002,399
Patent No. 8,250,295 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and
JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF CASE

Requester made a request for *inter partes* reexamination of U.S. Patent No. 8,250,295 B2 (“the ’295 patent”) issued to Hossein Amidi, Kelvin A. Marino, and Satyadey Kolli, entitled *Multi-Rank Memory Module that Emulates a Memory Module Having a Different Number of Ranks*. The ’295 patent issued August 21, 2012 and is assigned to Patent Owner, SMART Modular Technologies, Inc.

Requestor requested reexamination of claims 1–7 of the ’295 patent. Request 4.¹ Claim 8 is not subject to reexamination. RAN 1. During the proceeding, claims 9–24 were added, and subsequently claims 10–12, 14, 16–18, 20, 21, 23, and 24 were canceled. RAN 2; App. Br. 1. The Examiner confirmed claims 1–7 and determined claims 9, 13, 15, 19, and 22 to be patentable. RAN 1 and 5; App. Br. 1. No rejections are pending. RAN 1.

Requester appeals under 35 U.S.C. §§ 134(b) and 315 (2002) (pre-AIA) from the decision in the RAN not to adopt various rejections. App. Br. i. Patent Owner filed a respondent brief, and Requester filed a rebuttal brief. Resp. Br.; Reb. Br.

The Examiner’s Answer relies on the RAN, incorporating it by reference. *See* Ans. 1.

An oral hearing was conducted on September 22, 2016. A transcript will be made of record.

¹ Throughout this opinion, we refer to (1) the Appeal Brief (“App. Br.”) filed by Requester, (2) the Respondent Brief filed by Patent Owner (“Resp. Br.”), (3) the Rebuttal Brief filed by Requester (“Reb. Br.”), (4) the Examiner’s Answer (“Ans.”), (5) the Examiner’s Right of Appeal Notice (“RAN”), (6) the Action Closing Prosecution (“ACP”), and (7) Requester’s request for reexamination (“Request”).

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We have been informed that the '295 patent (1) is the parent application for U.S. Application No. 12/902,073² and (2) is the subject of litigation, which has been stayed in view of this reexamination proceeding.³ App. Br. 1. Requester also informs us that Patent Owner has sought an interference with U.S. Patent No. 7,619,912, which is currently being reexamined in the merged *inter partes* reexamination proceedings assigned Control Nos. 95/001,339, 95/000,578 and 95/000,579.⁴

We have jurisdiction under 35 U.S.C. §§ 134(b) and 315.

We REVERSE the Examiner's decision to confirm claims 1–7 and to determine claims 9, 13, 15, 19, and 22 are patentable.

Original claim 1 reads as follows:

1. A memory module connectable to a computer system, the memory module comprising:
 - a board;
 - a plurality of double-data-rate (DDR) memory devices mounted to the board, the plurality of DDR memory devices arranged in a first number of ranks;
 - a circuit that is coupled to said board and that receives from the computer system a set of input control signals that includes a set of first chip select signals and an address signal and that generates a set of second chip select signals based at least in part upon values of said set of first chip select signals and a portion of the address signal;

² This application is currently suspended by the Office.

³ *SMART Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 12-cv-2319 (C.D. Cal.).

⁴ The Board rendered a Decision on Appeal in the merged reexamination proceedings on May 31, 2016. *Inphi Corp. et al v. Patent of Netlist, Inc.*, 2016 WL 3088406 (PTAB May 31, 2016). Patent Owner requested to reopen prosecution on August 1, 2016 in response to new grounds of rejection set forth in the Decision on Appeal. Requester also requested rehearing on June 30, 2016.

wherein a number of chip select signals of the set of second chip select signals corresponds to a first number of DDR memory devices arranged in the first number of ranks;

wherein a number of chip select signals of the set of first chip select signals corresponds to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks;

wherein at least one signal of the set of second chip select signals has a value to selectively activate a respective rank of the first number of ranks;

wherein the circuit provides one or more of the received set of input control signals to said at least one respective activated rank;

wherein the set of input control signals further includes RAS, CAS, WE, BA;

wherein the circuit includes an emulator and a register; and

wherein the emulator receives from the computer system at least a portion of the set of input control signals that includes RAS, CAS, WE, the set of first chip select signals and the portion of the address signal;

wherein the emulator generates the set of second chip select signals in response to the at least a portion of the set of input control signals received by the emulator;

wherein the register receives at least another portion of the set of input control signals that includes RAS, CAS, WE, BA and the remaining portion of the address signal; and

wherein the register provides one or more of the input control signals received by the register to said at least one respective activated rank.

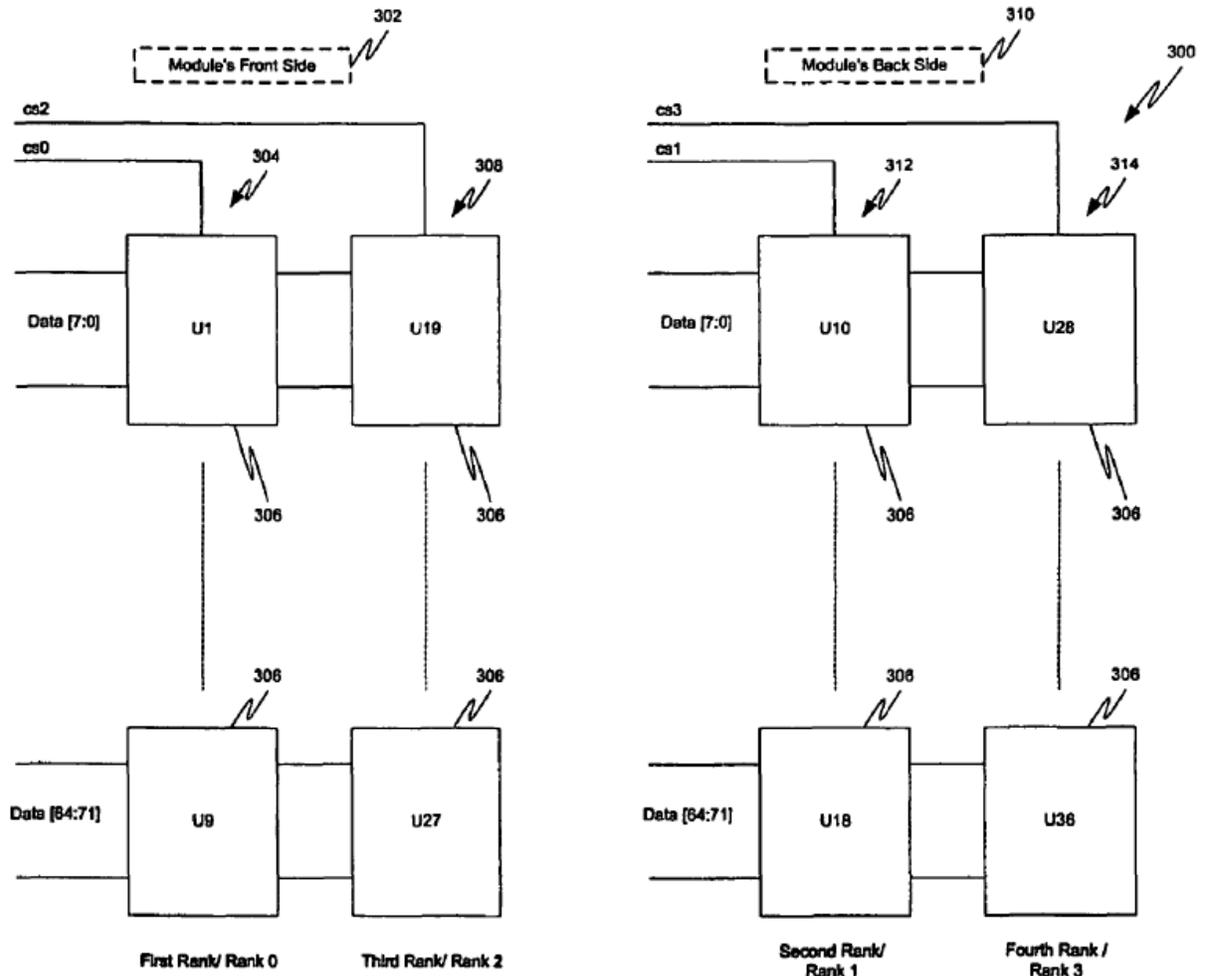
App. Br. 39–40, Claims App.

A. The Invention

The '295 patent “relates to computer memory. More particular, the present invention relates to a four rank memory module.” The '295 patent 1:7–9. The '295 patent states “[a] need . . . exists for a transparent four rank memory module fitting into a memory socket having two chip select signals routed. A primary

purpose of the present invention is to solve these needs and provide further, related advantages.” The '295 patent 2:47–50.

An example of a transparent four rank memory module is shown in Figure 3 below:

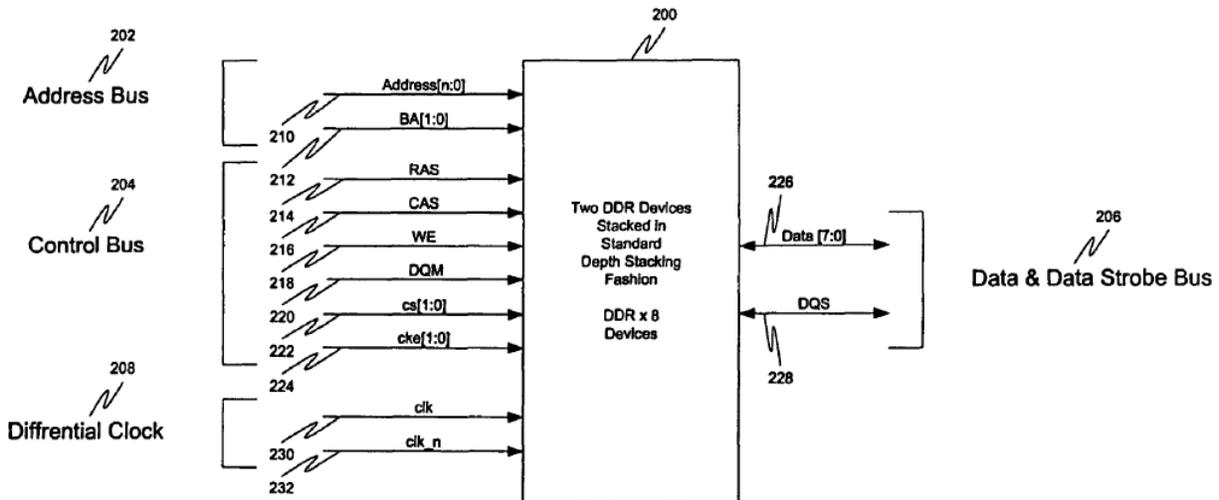


Transparent Four Rank DDR Module Block Diagram
 FIG. 3

The '295 patent 3:10–12. Figure 3 shows stacked DDR 8-bit memory devices 306 on the front and back side of memory module 300. *Id.* at 4:33–35, Fig. 3. Two ranks of memory devices (*e.g.*, 304, 308) are located on the module’s front side and two ranks of memory devices (*e.g.*, 312, 314) are located on the module’s back

side. *Id.* at 4:36–39, 47–50, Fig. 3. A chip select signal (*e.g.*, cs0–cs3) is coupled to each rank of memory devices. *Id.* at 4:43–46, 53–57, Fig. 3.

In contrast, a standard two rank memory module shown in Figure 2 below has only two chip select signals, cs[1:0]:

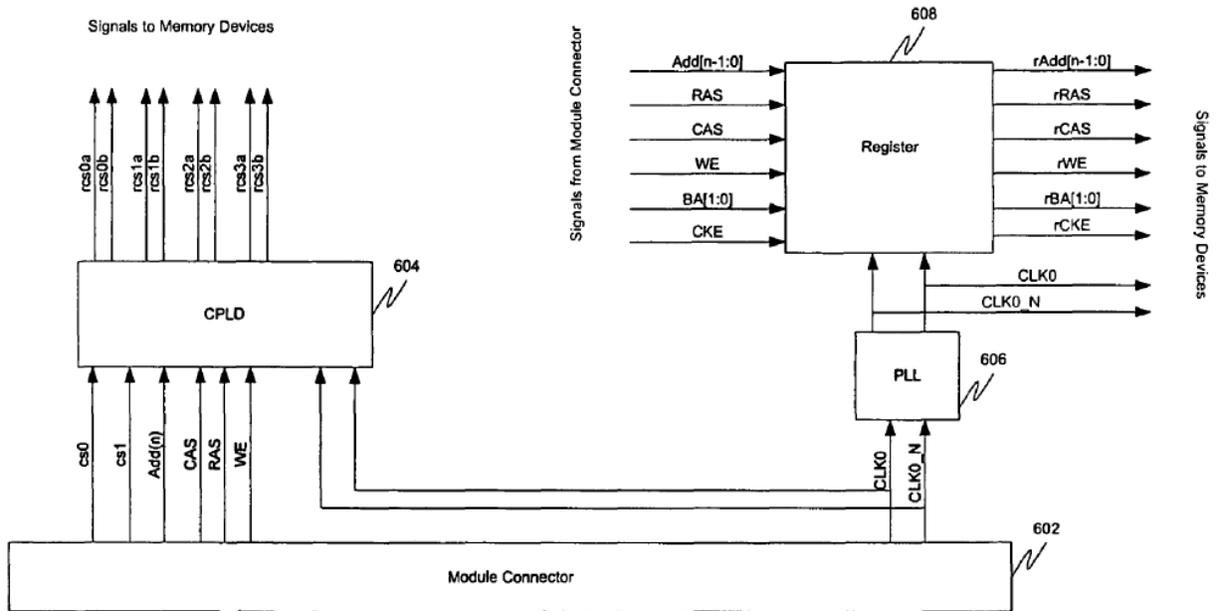


Standard DDR Device Depth Stacking Block Diagram

FIG. 2

The '295 patent 4:59–61, Fig. 2. Specifically, memory device 200 interfaces with a memory controller (not shown) and three buses, one of which is control bus 204. *Id.* at 4:20–22, Fig. 2. The control bus conveys signals, including cs[1:0] 222, which are the two chip select signals. *Id.* at 4:26–28, 59–61, Fig. 2.

Figure 3, shown above, allows its four-rank memory module to communicate with a memory socket having only two chip select signals routed, like that shown in Figure 2. *See id.* at 4:61–64. For example, Figure 6A, depicted below, shows the row decoding process of a transparent four rank memory module that includes complex programmable logic device (CPLD) 604:



Row Address Decoding
 FIG. 6A

The '295 patent 3:22–25, 6:57–58, Fig. 6A. CPLD 604 “ensures that all commands for a two rank memory module conveyed by the module connector 602 are also performed on the four rank memory modules. For example, CPLD 604 generates $rsc2$ and $rsc3$, besides $rsc0$ and $rsc1$ off of $CS0$, $CS1$ and $Add(n)$ from the memory controller side.” *Id.* at 7:10–15, Fig. 6A.

The '295 patent also states

Those of ordinary skill in the art will realize that the following detailed description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the present invention will readily suggest themselves to such skilled persons having the benefit of this disclosure.

The '295 patent 3:39–44.

Also, the '295 patent concludes:

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Many other families of memory devices or densities of memory devices (not shown) may be used to build the four rank memory module. Those of ordinary skill in the art will appreciate that the example of four rank memory module described above is not intended to be limiting and that other configuration can be used without departing from the inventive concepts herein disclosed.

The '295 patent 9:39–45.

B. Cited Prior Art

Requester relies on the following as evidence of unpatentability:

Watanabe	US 5,463,590	Oct. 31, 1995
Matsui	US 5,953,280	Sept. 14, 1999
Takeda	JP H10-320270	Dec. 4, 1998

JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Release 11b, Rev. 1.3*, pages 4.20.4-1–4.20.4-82 (Jan. 2002) (“JEDEC 21-C”)

JEDEC Solid State Technology Association, *JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79C (Revision of JESD79B)* 1–75 (Mar. 2003) (“JEDEC 79C”)

Hynix Semiconductor, *128Mx72 bits Registered DDR SDRAM DIMM HYMD512G726(L)8-K/H/L Rev 0.1*, pages 1–16 (May 2002) (“Hynix”).

Admitted Prior Art in the '295 patent, 2:16–19, stating it is known that memory devices with lower densities are cheaper and more readily available and it may be advantageous to build a memory module using lower density devices (“APA”).

The following Declarations are presented in this proceeding:

Declaration of Dr. Edward P. Sayre dated April 25, 2013 (Sayre Decl.) and

Declaration of William Slemmer dated March 26, 2013 (Slemmer Decl.)

C. Proposed Non-Adopted or Withdrawn Rejections

The Requester appeals the Examiner’s decision not to reject various claims based on the following proposed rejections:

Reference(s)	Basis	Claims	Last presented
Takeda and JEDEC 21-C (Ground 1)	§ 103(a)	1–7	Non-Final Act. 5–17
Takeda and Hynix (Ground 2)	§ 103(a)	1–7	Non-Final Act. 17–27
JEDEC 21-C, APA, and Matsui (Ground 3)	§ 103(a)	1–7	Non-Final Act. 27–38
Hynix, APA, and Matsui (Ground 4)	§ 103(a)	1–7	Non-Final Act. 38–48
JEDEC 21-C, APA, and Watanabe (Ground 5)	§ 103(a)	1–7	Non-Final Act. 49–58
Hynix, APA, and Watanabe (Ground 6)	§ 103(a)	1–7	Non-Final Act. 59–68
Takeda, JEDEC 21C, and JEDEC 79C (Ground 7)	§ 103(a)	9, 13, 15, 19, 22	3PR Comments 36–37 ⁵
JEDEC 21C, APA, Matsui, and JEDEC 79C (Ground 8)	§ 103(a)	9, 13, 15, 19, 22	3PR Comments 37–38
JEDEC 21-C, APA, Watanabe, and JEDEC 79C (Ground 9)	§ 103(a)	9, 13, 15, 19, 22	3PR Comments 38–39
(Ground 10)	§ 112(a)/¶ 1	9, 13, 22	3PR Comments 27–29

App. Br. 2–3, 9.

⁵ Requester’s Comments submitted April 26, 2013 (“3PR Comments.”)

II. ISSUES ON APPEAL

We review the appealed rejections for error based upon the issues identified by Requester in its appeal brief, and in light of the arguments and evidence produced thereon. *Cf. Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) (citing *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992)). “Any arguments or authorities not included in the briefs permitted under this section or [37 C.F.R.] §§ 41.68 and 41.71 will be refused consideration by the Board, unless good cause is shown.” 37 C.F.R. § 41.67(c)(1)(vii).

Based on the disputed errors presented by Requester, the main issues on appeal are whether the Examiner erred in:

A. determining “a set of first chip select signals” in independent claim 1 under the broadest reasonable construction means multiple chip select signals and

B. confirming claim 1 based on the proposed rejections of (1) Takeda and JEDEC 21-C or (2) Takeda and Hynix?

III. ANALYSIS

A. Claim Construction

During examination of a patent application, a claim is given its broadest reasonable construction “in light of the specification as it would be interpreted by one of ordinary skill in the art.” *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (internal citations and quotations omitted). We presume that claim terms have their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (internal quotations omitted) (“The ordinary and customary meaning ‘is the meaning that the term would have to a person of ordinary skill in the art in question.’”). However,

patentees may rebut this presumption by acting as their own lexicographer, providing a definition of the term in the specification with “reasonable clarity, deliberateness, and precision.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

A Set of First Chip Select Signals

One major issue of this appeal centers around the broadest, reasonable construction of the term “set” in the context of the entire phrase “a set of first chip select signals” recited in claim 1. Requester argues that the term “set” for this recitation should be interpreted as one or more chip select signals. App. Br. 10–21; Reb. Br. 1–11. The Examiner and Patent Owner counter that the recited “set” means a collection of multiple items and thus, the recited “set of first chip select signals” means a collection of multiple first chip select signals. *See* ACP 10; Resp. Br. 2–11. Upon considering all the arguments and evidence of record, we agree with the Examiner and Patent Owner.

The word “set” in claim 1 is used to recite three, distinct signal groups. Resp. Br. 3. Claim 1 recites “a set of input control signals,” “a set of first chip select signals,” and “a set of second chip select signals.” The ’295 patent 9:61–10:2. The remaining recitations of the sets in claim 1, which according to the Examiner and Patent Owner appear fourteen times (*see* ACP 9; Resp. Br. 2–3), claim these three, distinct “sets” in more detail.

As noted by the Examiner and Requester, the recitations to the “set of input control signals” and the “set of second chip select signals” claim or identify multiple signals. ACP 9–10; Resp. Br. 3–5. For example, the Examiner discusses (ACP 9) that the “set of input control signals” includes “a set of first chip select signals,” an address signal, and further includes RAS, CAS, WE, and BA. The

'295 patent 9:61–10:1 and 10:21–22. The claim also recites portions of the input control signals (the '295 patent 10:25–27 and 31–33), further indicating that the recited “set” of input control signals is more than one signal.

As a second example, the number of chip select signals of the “set of second chip select signals” corresponds to a first number of DDR memory devices, the number of chip select signals of the “first chip select signals” corresponds to a second number of DDR memory devices, and the number of second DDR memory devices is smaller than the first number of DDR devices. The '295 patent 10:5–12. As such, the “set of second chip select signals” must include multiple signals, because the recited number of first chip select signals is smaller than the number of second chip select signals and at least one first chip select signal must be claimed for the phrase of “a set of first chip select signals” reasonably to have meaning. *See* ACP 9; *see* Resp. Br. 8–9. Additionally, claim 1 recites “at least one signal of the set of second chip select signals” (the '295 patent 10:15–16), which further implicitly claims the set of second chip select signals includes more than one signal. *See* Resp. Br. 4.

To be sure, claim 1 does not identify specific, multiple signals included in the “set of first chip select signals” in claim 1. App. Br. 11; Reb. Br. 2. Because of this difference in claim 1, Requester urges the “set of first chip select signals” to be construed differently than the other recited (a) “set” of input control signals and (b) “set” of second chip select signals to encompass *one* or more first chip select signals. App. Br. 11.

Requester asserts the word “set” in claim 1 is construed consistently and reasonably to be one or more things. *See* App. Br. 10–11. In particular, in the case of the “set of input control signals” and the “set of second chip select

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signals,” Requester contends these sets are limited to multiple signals by the additional limitations in claim 1 and not by the word “set.” *See id.*; *see* Reb. Br. 3–4. On the other hand, Requester asserts the recited “set” in the context of the first chip select signals is not so limited. App. Br. 11; Reb. Br. 2.

Turning to the disclosure to assist in our understanding, Requester argues the ’295 patent supports construing “set” as a collection of one or more things. App. Br. 14–16. Initially, we note that the only passage of the ’295 patent that discusses a “set,” other than the claims, is in the context of address lines and memory. The ’295 patent 8:41–44. However, this passage does not provide reasonable clarity or precision such that the term “set” is defined and further does not assist in understanding the term in the context of the recited first chip select signals. *See id.*

The Examiner states that every embodiment in the disclosure of the ’295 patent has two chip select signals (*e.g.*, cs0, cs1). ACP 10 (citing the ’295 patent 4:26–28, 5:57–6:7, 6:57–67, 8:5–15, 37–48; Figs. 2, 5, 6A–B); *see also* Resp. Br. 7. However, courts have “rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment.” *Philips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005). In fact, although the language in the ’295 patent may be “boilerplate” (Resp. Br. 8; Reb. Br. 5–6), the ’295 patent states the description is “illustrative” and contemplates other embodiments. The ’295 patent 3:39–44, 9:39–45.

On the other hand, the court in *In re Abbott Diabetes Care Inc.*, 696 F.3d 1142 (Fed. Cir. 2012) determined that the recitation to “an electrochemical sensor . . . having a plurality of contact pads” and configured “for coupling to” the conductive contacts, excludes sensors that have external cables and wires. *See*

id. at 1149. In particular, the court determined the claims themselves suggest connectivity without the inclusion of cables or wires. *See id.* Similarly, as discussed above, claim 1 suggests “a set” is two or more items.

Additionally, the court in *Abbott Diabetes* found, even though the disclosure had no explicit statement disclaiming electrochemical sensors with external cables or wires, every embodiment disclosed in the specification showed the sensor without external cables and wires and thus by implication defines the “electrochemical sensor” to be a sensor without external cables or wires. *See Abbott Diabetes*, 696 F.3d at 1149–50. Similarly and as noted by the Examiner and Patent Owner (ACP 10; Resp. Br. 7), the disclosure does not contain an explicit statement disclaiming the “set” of first chip select signals with one signal, but every embodiment of the set of first chip select signals discussed includes two first chip select signals and, by implication, limits the “set” to more than one signal. *See* the '295 patent 4:26–28, 5:57–6:7, 6:57–67, 8:5–15, Figs. 2, 5, 6A–B.

In contrast with *Abbott Diabetes*, the disclosure of the '295 patent does not contain disparaging remarks. *See id.*, 696 F.3d at 1149. That is, the '295 patent has no explicit remarks disparaging the phrase “set of first chip select signals” from being a single chip select signal. *See generally* the '295 patent. Even so, the '295 patent states that systems typically have two memory chip selects routed per socket and that all standard memory modules have only two chip select signals per memory module routed. The '295 patent 1:29–31, 2:43–45. The '295 patent further states common memory modules have two chip select signals (one per rank) or four chip select signals (two per rank). The '295 patent 1:31–33.

These discussions suggest the recited “set of first chip select signals” are two or four and not a single first chip select signal as argued. Reb. Br. 6.

Granted, as Requester indicates, the ’295 patent discusses standard memory modules have either one or two ranks. The ’295 patent 1:41–42, *cited in* Reb. Br. 6. Requester argues this demonstrates the ’295 patent contemplates a “1-to-2 decoder” that generates two chip select signals from one chip select signal. App. Br. 15; Reb. Br. 4. However, Patent Owner notes that this discussion is in the Background section of the ’295 patent to describe standard memory modules that are known without discussing the corresponding number of chip select signals. Resp. Br. 8. Also, acknowledging in the ’295 patent that one rank memory modules were known does not demonstrate readily that the claimed invention contemplated a single chip select signal as the “set of first chip select signals.” Furthermore, the discussion in JEDEC 21-C (App. Br. 15) concerns Dual In-line Memory Modules (DIMMs) populated as “one physical bank” (JEDEC 21-C, p. 4.20.4-10). To the extent the DIMM receives a single chip select signal, this still does not demonstrate readily that the claimed invention contemplated a single chip select signal as the “set of first chip select signals.”

Moreover, the prosecution history of the ’295 patent, including changing the title of the ’295 patent, does not change the meaning of “set” in the claims as argued. App. Br. 16–18; Reb. Br. 8–10. Granted, the title was broadened from “Transparent Four-Rank Memory Module For Standard Two Rank Sub-systems” to “Multi-Rank Memory Module that Emulates a Memory Module Having a Different Number of Ranks.” App. Br. 17; Reb. Br. 9. However, this change does not demonstrate persuasively that “a set” in the claims has enlarged to

include one first chip select signal. *Cf. In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004). Rather, as explained above, the broadest, reasonable construction of “a set of first chip select signals” in light of this amendment can encompass two *or more* first chip select signals.

Requester further asserts that the differing language in claim 1 demonstrates that the recitation to “a set” for the first chip select signals should be construed as one or more items. App. Br. 12–14; Reb. Br. 3–4. In particular and relying on *Bancorp Services, L.L.C. v. Hartford Life Insurance Co.* 359 F.3d 1367, 1373 (Fed. Cir. 2004), Requester contends the close-in-proximity language of “a *plurality* of double-data-rate (DDR) memory devices” (emphasis added) and “a *set* of first chip select signals” (emphasis added) should be construed distinctly and different in scope. App. Br. 12–13. That is, “a plurality” should be construed as two or more, whereas “the term ‘set’ is more flexible in its meaning than ‘plurality’” (Reb. Br. 3) allowing “a set” to be construed as one or more. App. Br. 12–13. When construing claim 1 in its entirety, we are not persuaded.

As noted by Patent Owner (Resp. Br. 4–5), *Bancorp* indicates that the use of different terminology does not conclusively demonstrate that terms should be construed differently. *Bancorp*, 359 F.3d at 1373. In particular, “it is not unknown for different words to be used to express similar concepts, even though it may be poor drafting practice.” *Id.* For example, the phrase “plurality” or “at least two” are different words that express similar concepts. Likewise, the words “set” and “plurality” express similar concepts for reasons discussed previously. Thus, even if the terms “set” and “plurality” are considered to be close in proximity, they can be construed similarly.

Requester even further argues that by the principle of claim differentiation the recitation to “a set of first chip select signals” must be broader in scope than dependent claim 6 (App. Br. 13–14; Reb. Br. 4–5), which recites “the set of first chip select signals consists of two signals” (the ’295 patent 10:52–53). This argument is unavailing. We agree that claim 1 is broader in scope than claim 6 but disagree that “claim 1 plainly reads . . . as no indication of multiple items” (Reb. Br. 4). To illustrate, claim 1’s scope can be reasonably construed such that the number of first chip select signals encompasses two signals *or more*, whereas claim 6 limits the first chip select signals to a specific number — two first chip select signals.

Concerning the declarations of Dr. Sayre and Mr. Slemmer, each takes conflicting positions how one skilled in the art would have understood the phrase “a set of first chip select signals” in light of the disclosure. *Compare* Sayre ¶¶ 23–25 *with* Slemmer Decl. ¶¶ 10–15. Dr. Sayre points to the same passage in column 1 of the ’295 patent and JEDEC 21-C as discussed above in concluding that a “set” is one or more signals. Sayre Decl. ¶¶ 23–24. We are not persuaded for the above reasons. On the other hand, Mr. Slemmer determines the word “set” in claim 1 has its ordinary meaning of a collection of two or more items. Slemmer Decl. ¶¶ 10, 13, 15. The Examiner further supports this meaning, introducing an ordinary meaning of “set” to include “any collection of objects.” ACP 10 (citing to Merriam-Webster’s Online Dictionary and Appendix A). We determine that Mr. Slemmer’s testimony related to how one skilled in the art would have understood the term “set” is reasonable, because the ’295 patent does not reflect that Patent Owner has acted as its own lexicographer to define a single signal as “a set of first chip select signals” and the record does not demonstrate

sufficiently that Patent Owner expressed an intent to deviate from the customary meaning of “set.”

Requester further asserts that the expert testimony and dictionary definitions are extrinsic evidence, which cannot prevail over the intrinsic evidence of the claim and the '295 patent's disclosure. App. Br. 12; Reb. Br. 7–8. We agree that this type of evidence may not be probative “in view of prevailing intrinsic evidence.” *Id.* (citing *Tempo Lighting, Inc. v. Tivoli, LLC*, 742 F.3d 973, 977 (Fed. Cir. 2014)). But in the instant case, the intrinsic evidence does not provide a definition of the term “set” or provide *prevailing* intrinsic evidence supporting Requester's position that “a set” include one or more items. Thus, looking to the customary meaning for an understanding of the term “set” is reasonable.

Accordingly, we determine that the broadest, reasonable interpretation “a set of first chip select signals” means multiple first chip select signals in light of the claims, the '295 patent's disclosure, the prosecution history of the '295 patent, the expert testimony of how one skilled in the art would have understood this term, and the ordinary meaning of the word “set.”

B. Confirmation of Claim 1

1. Takeda and JEDEC 21-C (Ground 1)

The Examiner confirms independent claim 1 based on the proposed rejection of Takeda and JEDEC 21-C because “Takeda discloses a single signal S0, S2 that is asserted on two separate lines.” ACP 13 (citing Slemmer Decl. ¶ 49). For this reason, the Examiner states Takeda does not disclose the recited “set of first chip select signals” and withdraws the rejection of claims 1–7 based on Takeda and JEDEC 21-C. ACP 13.

Requester disagrees with the Examiner's determination. App. Br. 21–27; Reb. Br. 11–14. Specifically, Requester argues that both (1) “a set of first chip select signals” in claim 1 includes one chip select signal and (2) one skilled in the art would have understood Takeda's S0 and S2 signals to be two chip select signals. App. Br. 21–27. Although we disagree with Requester that “a set of first chip select signals” includes one chip select signal (App. Br. 21–22), we agree that Takeda teaches “a set of first chip select signals”—namely two chip select signals—for the following reasons.

Takeda's Figure 2 is illustrated below:

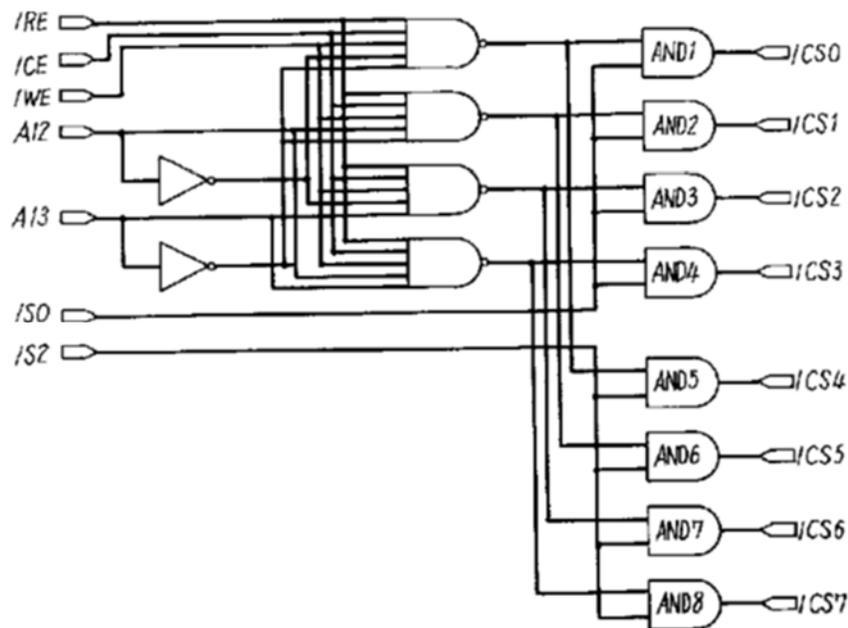


Figure 2 depicts a block diagram of the bank control unit.

Takeda ¶ 11. Figure 2 shows two inputs, /S0 and /S2, at the bottom left of the figure, each described as a drive signal from outside the module. The Examiner found and Patent Owner agrees that the /S0 and /S2⁶ inputs are actually one signal.

⁶ Although failing to use a nomenclature of “CS” to denote a chip select signal, Patent Owner does not dispute that “/S0” and “/S2” in Takeda are chip select

ACP 13; Resp. Br. 11–12. Specifically, Patent Owner acknowledges that there are two “separate (physical) wires” in Figure 2 but “wires are not the same as signals.” Resp. Br. 11. Patent Owner states “[e]quating wires with signals also does not make sense in the context of the claim language” of claim 1, which recites a circuit that receives control input signals, including the set of first chip select signals. Resp. Br. 12. Patent Owner contends Takeda receives a single chip select signal routed on two wires. *Id.*

Yet, Takeda describes the bank control unit as “converting drive signals from outside the module” into signals for controlling the banks. Takeda ¶ 11. Takeda discloses the bank control unit in Figure 2 receives drive signals “from outside the module” and converts them into signals for controlling banks. *Id.* Takeda discloses these outside, drive signals as “/RE, /CE, /WE, A12, A13 etc.” Takeda ¶ 12. Given that the only inputs in Figure 2 other than /RE, /CE, /WE, A12, and A13 are /S0, and /S2, we determine one skilled in the art would have appreciated /S0 and /S2 are the drive signals covered by “etc.” Moreover, to call each of RE, /CE, A12, and A13 in Takeda a drive signal but not each of /S0 and /S2 would be inconsistent. Also, /S0 and /S2 control different SDRAMs, further suggesting to ordinarily skilled artisan each input (e.g., /S0 and /S2) is a different signal. *See* Takeda, Fig. 2; *see also* App. Br. 22–23 and Reb. Br. 12. Dr. Sayre also reiterates these understandings (Sayre Decl. ¶ 56),⁷ while Mr. Slemmer provides no persuasive rebuttal. *See generally* Slemmer Decl.

signal(s). *See generally* Resp. Br. Additionally, Requester demonstrates a similar nomenclature is used JEDEC 21-C for chip select signals. App. Br. 24–25 (reproducing pages 4.20.4–8 and 4.20.4–16 with annotations).

⁷ Patent Owner has not challenged Dr. Sayre’s qualifications or that he is not qualified to address Takeda and what one of ordinary skill in the art would have

To counter this position, Mr. Slemmer states that it “is not unusual to have the same signal labeled differently on different unconnected lines in a circuit.” Slemmer Decl. ¶ 53. Mr. Slemmer contends this is done “to reduce loading due to fanout of the signal to multiple components.” *Id.* Mr. Slemmer also states that computer-assisted design (CAD) conventions do not allow for unconnected wires in the same diagram to have the same name even though the “wires have the same signal.” *Id.* For these reasons, Mr. Slemmer asserts that the same signal is given different names /S0 and /S2. *Id.* We are not persuaded.

First, Takeda does not discuss /S0 or /S2 are the result of fanning out a single signal to reduce loading. *See generally* Takeda. Rather, Takeda discloses each input as a drive signal as previously discussed. Nor does Takeda’s Figure 2, or any other figure for that matter, show the existing connections and circuitry prior to receiving the drive signals, such that Takeda illustrates the drive signals from outside the module are fanned out from a single signal. *See id.* That is, unlike /S0 and /S2 in Figure 2 showing their inputs divided into four separate lines entering gates, Takeda does not show /S0 and /S2 are similarly divided from a single signal. *See* Takeda, Fig. 2.

Second, although Mr. Slemmer may be correct that different lines in a circuit may require different nomenclature when using CAD applications (Slemmer Decl. ¶ 53), Dr. Sayre provides an equally plausible, alternative nomenclature that one skilled in the art would have adopted when naming a signal “stemming from the same input.” Sayre Decl. ¶ 50. Dr. Sayre illustrates his position, pointing to the ’295 patent’s use of “rcs0a” and “rcs0b” to indicate different names for the same

understood regarding Takeda. Likewise, Requester has not challenged Mr. Slemmer’s qualifications.

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signal. *Id.*; *see* the '295 patent, Figs. 6A and B. Patent Owner does not rebut this position by Dr. Sayre. *See generally* Resp. Br. Moreover, unlike Dr. Sayre, Mr. Slemmer provides no supporting evidence other than his opinion that one skilled in the art would have understood /S0 and /S2 are the same signal labeled differently on the unconnected lines in Takeda. Slemmer Decl. ¶¶ 49, 53, 56, 57 (the later three paragraphs stating “[i]t is my opinion”)

Third, Requester further provides an industry standard document, JEDEC 21-C, addressing a specific DDR Synchronous Dynamic Random Access Memory (SDRAM) DIMM having two physical banks. App. Br. 23–24 (reproducing an annotated block diagram of page 4.20.4–16); *see* Reb. Br. 12. Although Requester has not demonstrated that Takeda’s SDRAMs and register are the same or similar to the DIMM shown on page 4.20.4–16 in JEDEC 21-C, JEDEC 21-C provides some evidence that separate chip select signals, $\bar{S}0$ and $\bar{S}1$, use similar nomenclature to Takeda to designate separate chip select signals entering and exiting a register. To this evidence, Patent Owner provides insufficient rebuttal. Resp. Br. 11–12.

As asserted by Patent Owner (Resp. Br. 11), /S0 and /S2 have the same value as shown below in Takeda’s Figure 3.

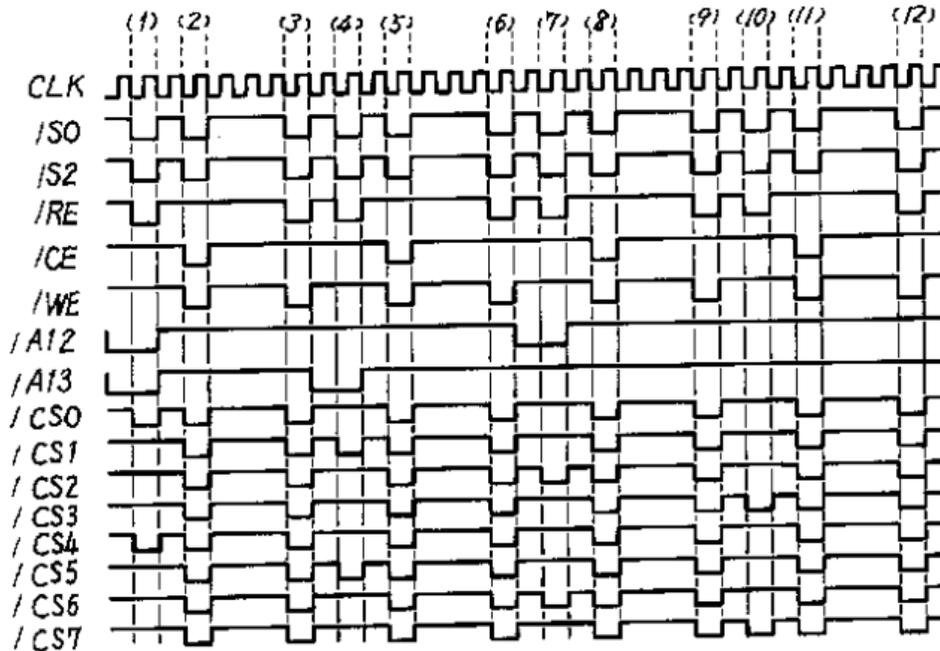


Figure 3 depicts a timing chart of the Figure 2 bank control unit's operations. Takeda ¶ 11. To the extent Patent Owner is arguing that each of these inputs are the same signal because /S0 and /S2 have the same value (*see* Resp. Br. 11–12), we find this argument unavailing.

We agree that Figure 3 above shows twelve periods (*i.e.*, (1)–(12)) from left to right at the top of the figure where /S0 and /S2 have the same value through its cycle. *See* Takeda, Fig. 3. Even so, two signals having the same value does not persuasively demonstrate that the signals are in fact a single chip select signal; rather, they are two chip select signals which have the same value in the timing chart of Figure 3. *See* Reb. Br. 12. Moreover, Takeda demonstrates one embodiment of a bank control unit. There is no persuasive evidence to demonstrate that Takeda fails further to suggest that /S0 and /S2 cannot have different values.

Requester additionally argues that Takeda suggests duplicating a single chip select signal would have been well-known and conventional. App. Br. 26–27; Reb. Br. 13–14. Patent Owner disagrees. Resp. Br. 12–13. Because we determine that Takeda teaches or suggests two first chip select signals as explained above, we do not reach this alternative position.

Given the record, we determine Takeda teaches two chip select signals (i.e., /S0 and /S2) that reasonably map to “a set of first chip select signals” as recited.

Patent Owner also argues that Takeda does not teach the recited “set of second chip select signals.” Resp. Br. 13–14. Patent Owner contends that “the activation of a single group of SDRAM from among four groups of SDRAM [is] controlled entirely by the A12, A13 inputs” and that /S0 and /S2 “merely act[] to select all of the SDRAMs of the four groups in unison during provision of active A12, A13 signals and to unselect all of the SDRAMs of all four groups in unison when A12, A13 are not active.” Resp. Br. 13. Patent Owner also argues the signals, /RE, /CE, and /WE are used to identify the bank active commands but not to select the bank to activate. Resp. Br. 14. For support, Patent Owner discusses various paragraphs in Takeda and Mr. Slemmer’s testimony. *Id.* (quoting Takeda ¶ 12 and citing Takeda ¶¶ 13 and 15 and Slemmer Decl. ¶ 58).

Given the breadth of claim 1, we are not persuaded. Claim 1 recites “a circuit . . . that generates a set of second chip select signals based at least in part upon values of said set of first chip select signals and a portion of the address signal.” As recited, the second chip select signals are *based on* values of the first chip select signal set. There is no further limitation in claim 1 that the first chip select signals’ values are used in any particular fashion to arrive at the second chip select signals, such as that shown in Figure 5’s truth table of the ’295 patent. *See*

the '295 patent, Fig. 5. Nor does claim 1 require that the first chip selects are used to select a bank or rank to activate. Rather, claim 1 further recites “at least one signal of the set of second chip select signals has a value to selectively activate a respective rank”—not that the first chip select signals’ values are used to select the bank or rank to activate as argued and testified. App. Br. 14; *see* Slemmer Decl. ¶ 58.

Granted, Takeda discusses specifically using signals, /RE, /CE, and /WE to identify SDRAM bank active commands, and /RE, /CE, /WE, decoded A12, and decoded A13 to perform bank selection. Takeda ¶¶ 12–13. However, as noted above, claim 1 does not require /S0 or /S2, the first chip select signals, be involved in identifying bank active commands or performing bank selection. Rather, at least one second chip select signal’s value, as recited, is used to activate selectively a respective rank.

Additionally, although /S0 and /S2 only “act[] to select all the SDRAMs” (Resp. Br. 13), this alleged selection using the first chip select signals’ values is involved in the bank/rank activation process, including generating the set of second chip select signals, at least one of which is used to active a respective bank as recited. That is, although “[t]here is no mention of signal[s] S0, S2 in the []listed passages from Takeda” (Resp. Br. 14), Takeda’s Figures 2 and 3 support that its inputs (e.g., its values) are used in some fashion to generate the second chip select signals. *See* Takeda, Fig. 2 (where /S0 and /S2, along with the other signals, are inputted into AND gates and /CS0–/CS7 are generated as a result of those input signals); *see also* Sayre Decl. ¶ 57 (discussing Figure 3 uses the signals’ values in the timing chart to generate /CS0–/CS7). Requester similarly indicates that the /S0 and /S2 signals in Takeda are received and used to generate the second chip select

signals. *See* Reb. Br. 14 (citing Sayre Decl. ¶ 69). We thus determine that Takeda suggests that the second chip select signals (e.g., /CS0–/CS7) are *based at least in part* on the first chip select signals’ values. On balance, we agree with Requester that Takeda teaches “a set of first chip select signals” and “a set of second chip select signals” as recited.

As such, the Examiner erred in confirming claim 1.

Concerning the remaining, undisputed limitations of claim 1 and dependent claims 2–7, we adopt the Examiner’s rejection presented in the Non-Final Action and Requester’s proposed rejection presented in the Request. Non-Final Act. 5–17; Request 24–26, Ex. 18.

2. *Takeda and Hynix (Ground 2)*

The Examiner similarly confirmed claim 1 on Ground 2 for the same reasons as Ground 1. ACP 13. That is, in the Examiner’s view, Takeda teaches a single first chip select signal (e.g., S0, S2) instead of two separate first chip select signals /S0 and /S2. *Id.* For the above reasons, we disagree. Accordingly, the Examiner also erred in confirming claim 1 based on Ground 2 for reasons previously discussed. Concerning the undisputed limitations of claim 1 and dependent claims 2–7, we adopt the Examiner’s rejection presented in the Non-Final Action and Requester’s proposed rejection presented in the Request. Non-Final Act. 17–27; Request 27, Ex. 19.

3. *Takeda, JEDEC 21-C, and JEDEC 79C (Ground 7)*

Requester additionally proposed to reject claims 9, 13, 15, 19, and 22 based on Takeda, JEDEC 21-C, and JEDEC 79C. 3PR Comments 36–37. The Examiner

does not adopt this rejection for the same reasons as those discussed above concerning Ground 1 based on Takeda and JEDEC 21-C. *See* ACP 13; RAN 5–6. Based on the record, as explained above concerning Takeda and JEDEC 21-C, we determine the Examiner erred in determining claims 9, 13, 15, 19, and 22 are patentable. RAN 1. Regarding the undisputed limitations of claims 9, 13, 15, 19, and 22, we adopt the Requester’s proposed rejection presented in the Requester’s Comment on April 26, 2013. 3PR Comments 36–37, Ex. C.

4. *Written Description Rejection (Ground 10)*

Lastly, Requester argues that new claims 9, 13, and 22 should be rejected under 35 U.S.C. § 112, first paragraph. App. Br. 31–37; Reb. Br. 18–22. Requester asserts that the recitations of “a refresh command” or “precharge command” encompass undue breadth. App. Br. 31–37. Requester contends that there is distinction between an *auto* precharge command and its circuitry, which is reasonably conveyed by the ’295 patent’s disclosure, and the broader, recited phrase of “a precharge command.” App. Br. 31–35. Similar reasoning is presented concerning the recited “refresh command” differing from the disclosed *auto* refresh command in concluding the recitation “a refresh command” encompasses undue breadth. App. Br. 35–37.

To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. *See, e.g., Moba, B.V. v. Diamond Automation, Inc.*, 325 F.3d 1306, 1319 (Fed. Cir. 2003). Courts recognize that a “disclosure of a single species within a genus may be enough support for a claim directed to the genus.” *Bilstad v. Wakalopulos*, 386

F.3d 1116, 1124 (Fed. Cir. 2004). On the other hand, “a disclosure of a species does not always suffice to describe broadly claimed subject matter,” especially in an unpredictable field. *In re Curtis*, 354 F.3d 1347, 1356 (Fed. Cir. 2004). In particular, the knowledge of one skilled in the art and the level of predictability in the field must be considered in determining whether the written description requirement has been satisfied. *Bilstad*, 386 F.3d at 1126.

The Examiner considered Requester’s position but was not persuaded and did not adopt the proposed written description rejection. ACP 16. In arriving at this conclusion, the Examiner contends that it is improper to rely on JEDEC 79C “to define or redefine the [’295] patent’s term.” *Id.*; *see also* Resp. Br. 18. The Examiner determined that one skilled in the art would have understood the disclosed auto precharge and auto refresh command in the ’295 patent are “encompassed under” the recited phrases, “a refresh command” and “a precharge command,” using the broadest, reasonable construction. ACP 16. Patent Owner agrees with the Examiner contending that one skilled in the art would have understood the recitations “do not refer to an unduly broad genus covering virtually any type of precharge or refresh operation” but “can only refer to an ‘auto precharge’ and ‘auto refresh’ operation.” Resp. Br. 17.

Yet, the Examiner fails to consider fully the evidence concerning the knowledge of one skilled in art, particularly the competing evidence related to this knowledge. App. Br. 32 (quoting JEDEC 79C, page 20); *see also* Sayre Decl. ¶¶ 98–99. For example, Requester does not rely on JEDEC 79C to define or redefine the term “precharge” as the Examiner asserts (ACP 16) but rather uses this document to provide evidence of an ordinarily skilled artisan’s understanding of the recited phrase “a precharge command.” App. Br. 33 (stating “JEDEC 79C

demonstrates the *perspective* of a POSITA [person of ordinary skill in the art] reading the '295 disclosure”) (emphasis added); Reb. Br. 19.

Specifically, JEDEC 79C discusses two types of “PRECHARGE” are known in the art. JEDEC 79C, page 20. The first type is a “PRECHARGE” command described as a command used to deactivate an open row in a particular bank or all banks; the second type is an “AUTO PRECHARGE” feature without requiring an explicit command. *Id.* Thus, JEDEC 79C provides some evidence of what one skilled in art would have understood the term “precharge command” in the claims of the '295 patent to mean. Dr. Sayre’s testimony repeats this position. Sayre Decl. ¶ 98.

But, the '295 patent refers to auto precharge in a manner that differs from that of JEDEC 79C. In particular, the '295 patent discusses generating the second chip select signals when issuing “CS0 Auto Precharge all Banks Commands” and “CS1 Auto Precharge all Banks Commands.” The '295 patent 7:15–18, 8:28–31; *see also* the '295 patent 9:24–25. In contrast, JEDEC 79C describes the AUTO PRECHARGE as a feature *without an explicit command*. JEDEC 79C, page 20. Requester argues that the phrase “requiring an explicit command” has “specific, concrete, technical (not merely stylistic) meaning.” Reb. Br. 19. But, this is a mere assertion with no supporting evidence. Reb. Br. 19–20. Thus, there is some evidence that the '295 patent discusses an auto precharge command differently from those discussed in JEDEC 79C.

Even so, other evidence in JEDEC 79C demonstrates that there are several types of refresh commands known to one skilled in the art. JEDEC 79C, page 20. JEDEC 79C describes both an “AUTO REFRESH” command and a “SELF REFRESH” command. *Id.* Dr. Sayre also testifies regarding the auto refresh

command but not the self refresh. Sayre Decl. ¶ 99. As such, Requester has provided some evidence that the recited “refresh command” as understood by an ordinary skilled artisan may encompass either an auto refresh command or a self refresh command (JEDEC 79C, page 20), while the ’295 patent’s disclosure only describes an auto refresh command (the ’295 patent 7:18–20, 8:31–33, 9:218–20). The Examiner has not fully considered this evidence, demonstrating multiple and known refresh commands, and Patent Owner does not provide a persuasive rebuttal.

Additionally, these discussions by the Examiner (ACP 16) and Patent Owner (Resp. Br. 17–19) do not consider the level of predictability in the art involved in the ’295 patent and whether the memory module technology of the ’295 patent is a predictable art, such that the auto refresh species described in the ’295 patent may suffice to describe the broadly recited “refresh command.” As such, on the record, the ’295 patent’s disclosure of a single species of refresh commands (*e.g.*, the auto refresh command) within a genus (*e.g.*, all refresh commands) is not enough support for claim 9’s language directed to the genus of refresh commands. Similarly, there is not enough support for the language found in claims 13 and 22 concerning the “refresh command.”

Based on the evidence concerning the knowledge of one skilled in the art related to known refresh commands, the Examiner erred in not adopting the written description rejection of claims 9, 13, and 22.

5. Remaining Proposed Rejections

Our conclusion that the Examiner erred in confirming claims 1–7 and finding claims 9, 13, 15, 19, and 22 patentable based on the above rejections

renders it unnecessary to reach the propriety of the remaining proposed rejections. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984); *cf. In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009). *See also* 37 C.F.R. 41.77 (a) (“The Patent Trial and Appeal Board ... may affirm or reverse each decision of the examiner on all issues raised on each appealed claim”) and *Gleave*, 560 F.3d at 1338.

IV. CONCLUSIONS

Requester demonstrated that the Examiner erred in confirming claims 1–7 based on (1) Takeda and JEDEC 21-C and (2) Takeda and Hynix.

Requester demonstrated that the Examiner erred in determining claims 9, 13, 15, 19, and 22 are patentable based on Takeda, JEDEC 21-C, and JEDEC 79C.

Requester demonstrated that the Examiner erred in not adopting the written description rejection under 35 U.S.C. § 112, first paragraph of claims 9, 13, and 22.

We do not reach the propriety of the remaining proposed rejections.

V. TIME PERIOD FOR RESPONSE

Pursuant to 37 C.F.R. § 41.77(a), the above-noted reversal constitutes a new ground of rejection. Section 41.77(b) provides that “[a] new ground of rejection . . . shall not be considered final for judicial review.” That section also provides that Patent Owner, **WITHIN ONE MONTH FROM THE DATE OF THE DECISION**, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of the appeal proceeding as to the rejected claims:

- (1) *Reopen prosecution*. The owner may file a response requesting reopening of prosecution before the examiner. Such a response must be

either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both.

(2) *Request rehearing.* The owner may request that the proceeding be reheard under § 41.79 by the Board upon the same record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

In accordance with 37 C.F.R. § 41.79(a), the “[p]arties to the appeal may file a request for rehearing of the decision within one month of the date of: . . . [t]he original decision of the Board under § 41.77(a).” A request for rehearing must be in compliance with 37 C.F.R. § 41.79(b). Comments in opposition to the request and additional requests for rehearing must be in accordance with 37 C.F.R. § 41.79(c)–(d), respectively. Under 37 C.F.R. § 41.79(e), “[t]he times for requesting rehearing under paragraph (a) of this section, for requesting further rehearing under paragraph (c) of this section, and for submitting comments under paragraph (b) of this section may not be extended.”

An appeal to the United States Court of Appeals for the Federal Circuit under 35 U.S.C. §§ 141–144 and 315 and 37 C.F.R. § 1.983 for an *inter partes* reexamination proceeding “commenced” on or after November 2, 2002 may not be taken “until all parties’ rights to request rehearing have been exhausted, at which time the decision of the Board is final and appealable by any party to the appeal to the Board.” 37 C.F.R. § 41.81; *see also* MPEP §§ 2682, 2683 (8th ed., Rev. 8, July 2010).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

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Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

REVERSED
37 C.F.R. § 41.77(b)

FOR PATENT OWNER:

SCHWEGMAN LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

FOR THIRD-PARTY REQUESTERS:

MORRISON & FOERSTER, LLP
707 WILSHIRE BOILEVARD
LOS ANGELES, CA 90017