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EXAMINER
AISAKA, BRYCE M

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Please find below and/or attached an Office communication concerning this application or proceeding.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL
AND APPEAL BOARD

Ex parte TONG GAO and HENG-YI CHAO[1]

Appeal 2016–005586
Application 12/695,391
Technology Center 2800

Before BEVERLY A. FRANKLIN, MICHAEL P. COLAIANNI, and JENNIFER R. GUPTA, *Administrative Patent Judges*.

FRANKLIN, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Appellants identify the real party in interest as Synopsys, Inc.

Appellants request our review under 35 U.S.C. § 134 of the Examiner's decision rejecting claims 1, 3–8, 10–15, and 17–21. We have jurisdiction over the appeal under 35 U.S.C. § 6(b).

STATEMENT OF THE CASE

Claim 1 is illustrative of Appellants' subject matter on appeal and is set forth below:

1. A computer-implemented method for routing a set of nets in a circuit design, the method comprising:

partitioning the circuit design into a partition hierarchy, wherein higher levels in the partition hierarchy have larger partition sizes than lower levels in the partition hierarchy; and

routing a set of nets in the circuit design by, iteratively:

for each net in the set of nets, associating the net with a partition in the partition hierarchy that completely encloses the net's bounding box, wherein each net's bounding box encloses all pins of the net;

routing nets in increasing order of levels in the partition hierarchy, wherein nets associated with non-overlapping partitions are routed in parallel using one or more processors; and

adjusting bounding boxes of nets which need to be routed again;

wherein at least one net in the set of nets its assigned to a first partition in a first level of the partition hierarchy in one iteration and to a second partition in a second level is higher than the first level.

THE REJECTION

Claims 1, 3–8, 10–15 and 17–21 are rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

ANALYSIS

To the extent that Appellants has presented substantive arguments for the separate patentability of any individual claims on appeal, we will address them separately consistent with 37 C.F.R. § 41.37(c)(1)(vii).

Upon consideration of the evidence and each of the respective positions set forth in the record, we find that the preponderance of evidence supports the Examiner's findings and conclusion that the subject matter of Appellants' claims are unpatentable as being directed to non-statutory subject matter. Accordingly, we sustain the Examiner's rejection on appeal for the reasons set forth in the Final Office Action and in the Answer, and affirm, with emphasis below.

Appellants present arguments on pages 13–17 of the Appeal Brief, which we do not repeat herein. We are unpersuaded by such arguments for the reasons provided by the Examiner in the record, particularly as presented on pages 2–8 of the Answer, which we incorporate herein.

Appellants respond in the Reply Brief that their independent claims provide an improvement to another technology or technical field. Appellants argue that as illustrated in their Figure 1, and as explained in paragraphs 31–43 of the Specification, the integrated circuit (IC) design and fabrication technology includes multiple stages. Appellants submit that an improvement to one or more stages (e.g., the physical implementation stage

described in paragraph 39 is an improvement to the IC designing and fabricating technology or technical field. Appellants argue that page 8 in the Examiner's Answer mentions the Supreme Court case of *Diamond v. Diehr*. Appellants note that, in the same way the process claim 1 in *Diamond v. Diehr* provided an improvement to rubber curing technology or technical field (i.e., "another technology or technical field"), their independent claims provide an improvement to IC design and fabrication technology or technical field (i.e., "another technology or technical field"). Reply Br. 4.

However, in making the aforementioned arguments, Appellants overlook the valid point made by the Examiner on page 6 of the Answer. Therein, the Examiner explains that what Appellants dub as an improvement in IC design (involving the claimed steps of routing of nets) is within the realm of abstract ideas because these steps involve manipulation of mathematical relationships. Ans. 6–7. Also, the Examiner states that with specific regard to Appellants' argument that "routing a set of nets in circuit design" is clearly a specific application, the Examiner makes a valid point that the asserted "specific application" is really an "idea" on how to design a circuit, and the "idea" is run by algorithms in a generic computer. We thus agree with the Examiner that the claims fail to include any such element or combination of elements, amounting to "significantly more" than the abstract idea. We are thus unpersuaded of error in the Examiner's position in the record.

DECISION

The rejection is affirmed.

TIME PERIOD

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

ORDER

AFFIRMED