UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/387,522	01/27/2012	Hiroshi Goto	393654US99PCT	9120

22850 7590 03/02/2018

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
GONDARENKO, NATALIA A

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
03/02/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
tfarrell@oblon.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte HIROSHI GOTO AND TAKEAKI MAEDA

Appeal 2016-004396
Application 13/387,522
Technology Center 2800

Before CARL W. WHITEHEAD JR, HUNG H. BUI and SHARON FENICK, *Administrative Patent Judges*.

Per Curiam.

DECISION ON APPEAL

STATEMENT OF THE CASE[1]

Appellants are appealing the Final Rejection of claims 1–3 and 5–12 under 35 U.S.C. § 134(a). Appeal Brief 1. We have jurisdiction under 35 U.S.C. § 6(b) (2012).

We affirm.

---

[1] An oral hearing was held on November 28, 2017.

Introduction

The present invention relates to an interconnection structure including a semiconductor layer of a thin-film transistor and an Al alloy film connected directly to the semiconductor layer in this order from the side of a substrate, wherein the semiconductor layer is composed of an oxide semiconductor layer composed of an oxide semiconductor, and a method for manufacturing the same; and a display device including the interconnection structure.

Specification, ¶1.

Illustrative Claims

1. An interconnection structure including a semiconductor layer of a thin-film transistor and an Al alloy film connected directly to the semiconductor layer above a substrate in this order from a side of the substrate, wherein

the semiconductor layer is composed of an oxide semiconductor,

the Al alloy film contains Co in an amount of 0.2 to 2 atomic % and further contains at least one of Cu and Ge,

wherein the Al alloy film has been deposited on the substrate heated to at least 200°C,

a contact resistance of the interconnection structure including the semiconductor layer of the thin-film transistor and the Al alloy film connected directly to the semiconductor layer above the substrate is less than 1×10^{-2} $\Omega \cdot cm^2$, and

the contact resistance of the interconnection structure including the semiconductor layer of the thin-film transistor and the Al alloy film connected directly to the semiconductor layer above the substrate is lower after the Al alloy film is deposited on a substrate heated to at least 200°C than the contact resistance of the interconnection structure including the semiconductor layer of the thin-film transistor and the Al alloy film connected directly to the semiconductor layer above the substrate after the Al alloy film is deposited on a substrate at room temperature and subsequently heated to a temperature of at least 200°C.

> 11. A method for manufacturing the interconnection structure according to claim 1, the method comprising
>
> depositing the semiconductor layer and depositing the Al alloy film, wherein
>
> a part of the Co is deposited, or deposited and enriched, at an interface of the semiconductor layer and the Al alloy film connected directly thereto by:
>
> (a) setting a substrate temperature during the deposition of the Al alloy film to 200°C or higher; or
>
> (b1) setting a substrate temperature during the deposition of the Al alloy film to 200°C or higher, and
>
> (b2) performing a heat treatment at a temperature of 200°C or higher after the deposition of the Al alloy film.

Rejections on Appeal

Claims 1–3, 5–10 and 12 stand rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Gotou (U.S. Patent Application Publication 2009/0004490 A1; published January 1, 2009), Kawakami (U.S. Patent Application Publication 2007/0040172 A1; published February 22, 2007) and Ochi (U.S. Patent 8,384,280 B2; issued February 26, 2013). Final Action 2–9.

Claims 1–3 and 5–12 stand rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Gotou, Ochi and Gotou (U.S. Patent Application Publication 2009/0011261 A1; published January 8, 2009). Final Action 9–18.

ANALYSIS

Rather than reiterate the arguments of Appellants and the Examiner, we refer to the Appeal Brief (filed September 3, 2015), the Reply Brief (filed

March 16, 2016), the Answer (mailed January 21, 2016) and the Final Action (mailed April 9, 2015) for the respective details.

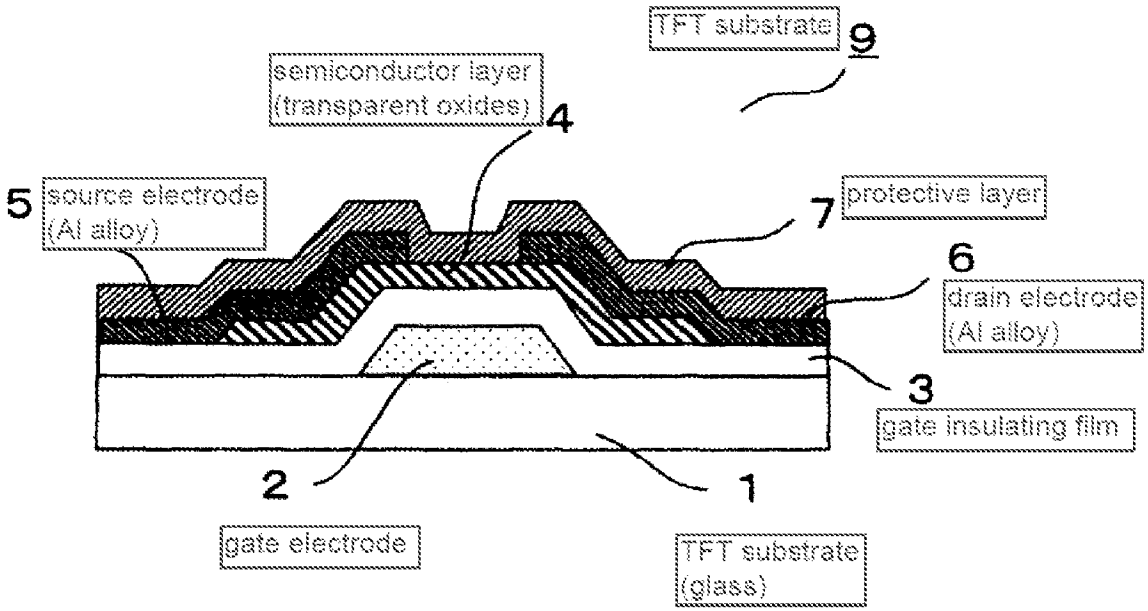
Claims 1–3, 5–10 and 12

Under the heading of "Claim Interpretation," Appellants contend the claimed interconnection structure has at least four significant limitations reproduced from claim 1:

> First, the Al alloy film of the claimed interconnection structure contains Co in an amount of 0.2 to 2 atomic % and further contains at least one of Cu and Ge.
>
> Second, the Al alloy film has been deposited on a substrate heated to at least 200°C.
>
> Third, the contact resistance of the interconnection structure including the semiconductor layer of the thin-film transistor and the Al alloy film connected directly to the semiconductor layer above the substrate is less than 1 x 10^{-2} $\Omega \cdot cm^2$.
>
> Fourth, the contact resistance of the interconnection structure including the semiconductor layer of the thin-film transistor and the Al alloy film connected directly to the semiconductor layer above the substrate is lower after the Al alloy film is deposited on a substrate heated to at least 200°C than the contact resistance of the interconnection structure including the semiconductor layer of the thin-film transistor and the Al alloy film connected directly to the semiconductor layer above the substrate after the Al alloy film is deposited on a substrate at room temperature and subsequently heated to a temperature of at least 200°C.

Appeal Brief 5.

We reproduce Appellants' Figure 1 below (annotated for clarity):



A TFT substrate 9 shown in Fig. 1 is of a bottom gate type and has a structure in which a gate electrode 2, a gate insulating film 3, a semiconductor layer 4, a source electrode 5/drain electrode 6, and a protective layer 7 are laminated successively from the side of a substrate 1.

Specification, ¶15.

Appellants argue:

> [T]he Examiner attributes no patentable significance whatsoever to Applicant's claim limitation that the contact resistance of Applicant's claimed interconnection structure must be lower after the Al alloy film is deposited on a substrate heated to at least 200°C than the contact resistance of the interconnection structure after the Al alloy film is deposited on a substrate at room temperature and subsequently heated to a temperature of at least 200°C.

Appeal Brief 6.

It is noted that Appellants cite several PTAB opinions throughout the Brief that are nonpresidential, and therefore, not binding on this panel. *See* Appeal Brief 6, 17 and 32.

Appellants argue the claimed device differentiates from the cited prior art device because:

> It should suffice to say that the evidence in Applicant's Specification shows that the properties of an interconnection structure with an Al-Co-(Cu/Ge) alloy layer deposited on a substrate heated to at least 200°C differ significantly from the properties of interconnection structures with an Al-Co-(Cu/Ge) alloy layer deposited on a substrate at room temperature, with or without subsequent heat treatment. If the properties of a product made by one process differ from the properties of a product made by another process, the products are not the same. *In re Papesch,* 315 F.2d 381 (CCPA 1963), instructs at 391, "[A] compound and all of its properties are inseparable; they are one and the same thing. If the properties of the products differ, the products are not, and cannot be, the same."

Appeal Brief 22 (emphasis added).

Appellants argue the claimed interconnection structure is different from the claimed invention by repeating the language from the claims and directing us to Tables 2 and 3 on pages 19 and 20 of the Specification. See Appeal Brief 15. These tables consist of multiple combinations of alloys, various temperatures and what appears to be galvanic corrosion resistance evaluation. See Specification 16, 19, 20. Appellants cite *Soni*'s direction that "when an applicant demonstrates *substantially* improved results . . . and *states* that the results were unexpected, this should suffice to establish unexpected results in the absence of evidence to the contrary. Appeal Brief 22 (quoting *In re Soni*, 54 F.3d 746, 750 (Fed. Cir. 1995) (emphasis from original text). In *Soni*, the applicants patent specification described "significantly improved properties" which were "much greater than would have been predicted." Soni, 54 F.3d at 747–48.

While Appellants have directed us to Tables 2 and 3 (Appeal Brief 15) these tables do not establish substantially improved results nor do they or the description of them in the Specification state that any results were unexpected. We have reviewed Appellants' Specification, and are not persuaded that Tables 2 and 3 and the associated sections of the Specification describing the contents of those tables describe "significantly improved properties" or establish unexpected results. The Reply Brief also fails to indicate support or evidence outside of Tables 1 and 2 to show unexpected results. See Reply Brief 5–6.

Gotou '261 discloses in paragraph 51 "for depositing an Al alloy film on a substrate, the temperature of the substrate is increased to the precipitation temperature of the alloy element or higher" and consequently, "the electric resistivity of the Al alloy can be reduced by the reduction of the alloy element content, and further, variations in contact electric resistance can also be remarkably controlled." Gotou '261 discloses that the manipulation of a substrate temperature can change the electric resistivity of a display apparatus having a structure in which a transparent oxide conductive film and an Al alloy film are in direct contact with each other on a substrate. *See* Gotou '261, ¶¶2, 56; Final Action 5–6.

"The patentability of a product does not depend on its method of production . . . If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe,* 777 F.2d 695, 697 (Fed. Cir. 1985)) (citations omitted). If the process limitation connotes specific structure and may be considered a structural limitation, however, that structure should be considered. *In re Garnero*, 412 F.2d 276,

279 (CCPA 1969) (holding that "interbonded one to another by interfusion" connotes structure to a claimed composite and should therefore be considered in the determination of patentability).

However, it is Appellants' burden to provide evidence establishing "an unobvious difference between the claimed product and the prior art product." *In re Marosi,* 710 F.2d at 803 (where a product-by-process claim is rejected over a prior art product that appears to be identical, although produced by a different process, the burden is upon the applicants to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product); *In re Best,* 562 F.2d at 1255, 195 USPQ at 433–34; *In re Brown,* 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972). Appellants have adduced no such evidence establishing "an unobvious difference between the claimed product and the prior art product." Nor have Appellants provided arguments or evidence that process limitations recited in claim that connote any specific structure.

For example, claim 1 recites an oxide semiconductor layer, an aluminum alloy film and a substrate. Claim 1's preamble states "an Al alloy film connected directly to the semiconductor layer above a substrate in this order from a side of the substrate." The contact resistance of the interconnection structure is not a component but merely a characteristic of the structure.

Moreover, claim 1 requires that " the Al alloy film has been deposited on the substrate;" however the "deposited on the substrate" does not indicate the Al alloy film is "directly connected" to the substrate in the same manner as the alloy layer is directly connected to the oxide layer because the claims are directed to a thin-film transistor interconnection structure where there are

intervening components between the substrate and the alloy layer such as the gate insulating film and the gate electrode. Claim 1's invention further calls into question the validity of Tables 2 and 3 demonstrating unexpected results because the tables do not account for structural characteristics such as thermal dissipation that occurs between the intervening components located between the alloy layer and the substrate.

Consequently, we do not find Appellants' arguments persuasive because the claimed invention is obvious in view of the cited art. *See Thorpe,* 777 F.2d at 697.

Claims 1–3, 5–12

Appellants contend:

> Claims 1–3 and 5–12 stand erroneously rejected under 35 U.S.C. § 103 over Gotou, WO 2009/081992 (published July 2, 2009), and Gotou '261 (OA, p. 9, ¶ 13). The Examiner cites Ochi (U.S. Patent 8,384,280, issued February 26, 2013) as an English translation of WO 2009/081992.
>
> The basic difference between these rejections and the rejections in the previous paragraph is that the Examiner here relies on [Gotou] WO 2009/081992, published July 2, 2009, as prior art. In the previous paragraph, the Examiner applied Kawakami to establish the claimed contact resistance of 1×10^{-2} $\Omega \cdot cm^2$ or less and relied on Ochi to show that Al-Co-X-(Z) alloy layers have properties and utility equivalent to Al-Ni-X-(Z) alloy layers in an interconnection structure. For the same reasons stated in response to the previous rejections, incorporated by reference here, the Examiner's rejections of Claims 1–3 and 5–12 for obviousness in view of Gotou, WO 2009/081992 (Ochi), and Gotou '261 also should be REVERSED.

Appeal Brief 23.

Thus, Appellants' arguments with respect to this rejection are based on the same distinctions related to the process of manufacture that we address above, and accordingly, we sustain the Examiner's rejection of claims 1–3 and 5–12 for the same reasons provided above.

Appellants provide additional arguments for dependent claim 11:

> [T]he patentability of dependent method Claim 11 over the applied prior art is separately argued because the method claim expressly requires manufacturing the interconnection structure according to claim 1 by depositing the semiconductor layer and depositing the Al alloy film, wherein a part of the Co is deposited, or deposited and enriched, at an interface of the semiconductor layer and the Al alloy film connected directly thereto by:
>
> (a) setting a substrate temperature during the deposition of the Al alloy film to 200°C or higher; or
>
> (b1) setting a substrate temperature during the deposition of the Al alloy film to 200°C or higher, and
>
> (b2) performing a heat treatment at a temperature of 200°C or higher after the deposition of the Al alloy film.
>
> The Examiner cannot simply disregard the express language of the claim and the unexpected comparatively lower contact resistance the evidence of record shows results therefrom. Claim language "should not [be] treated as meaningless." *Bicon, Inc. v. Straumann Co.,* 441 F.3d 945, 951 (Fed. Cir. 2006).

Appeal Brief 32.

It is noted that claim 11 is a method claim dependent upon the device claim 1 wherein the method of claim 11 is drafted in the alternative in which either step (a) is performed or step (b1) and (b2) are performed. The Examiner finds and we agree, that the combination of the prior art teaches or suggests step (a):

> **Appellant[s'] assertions are incorrect** because the Office Action dated 04/09/2015 [ ] **has addressed** the above limitations ***"wherein the Al alloy film has been deposited on the substrate heated to at least 200°C"*** using the secondary reference by [sic Gotou] **('261) that teaches the effect of substrate temperature at deposition on contact resistance,** specifically, **Gotou ('261) teaches forming the Al alloy at deposition temperature 250°C** (Gotou ('261), ¶0070-¶0074) and determining the contact resistance between the Al alloy film and the oxide film (ITO) (Gotou ('261), ¶0114), wherein the contact resistance of the Al-Ni alloy deposited on a substrate heated to 250ºC (Gotou ('261), ¶0103) is lower than the contact resistance of a reference sample manufactured by setting the substrate temperature at room temperature and followed by a heat treatment (Table 2 of Gotou ('261) ¶0119-¶0121). Thus, **a person of ordinary skill in the art would expect to have lower contact resistance when the Al alloy is deposited on a substrate heated to at least 200°C** than the contact resistance after depositing Al alloy on a substrate at room temperature and subsequently heated to a temperature of at least 200ºC. Further, the primary reference by [Gotou] discloses depositing the semiconductor layer (41/42/45) (Gotou, ¶0040, ¶0044, ¶0045) and depositing the Al alloy film (the source/drain and gate electrodes) (Gotou, Figs. 2, 4, ¶0046-¶0048), wherein the semiconductor layer is in direct contact with Al alloy (Gotou, ¶0044) and setting a substrate temperature during the deposition of the Al alloy film to 200ºC (Al alloy was formed at 200ºC) (Gotou, ¶0060); and the secondary reference by Ochi specifically teaches depositing the Al alloy film containing a Co (Ochi, Col. 7, lines 39–56) on the substrate having substrate temperature including 250ºC and further performing heat treatment. Thus, the combination [sic Gotou/Ochi/Gotou] ('261) discloses all limitations of claim 11.

Answer 19–20.

We have considered Appellants' additional arguments pertaining to dependent claim 11 and we are not persuaded of Examiner's error. We sustain the Examiner's obviousness rejection of dependent claim 11.

DECISION

The Examiner's obviousness rejections of claims 1–3 and 5–12 are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(v).

AFFIRMED