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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ROSS S. SCOULLER, FRANK K. BAKER JR.,
and RONALD J. SYZDEK

Appeal 2016-001366
Application 13/530,169[1]
Technology Center 2100

Before JOHNNY A. KUMAR, JOHN P. PINKERTON, and
JOHN D. HAMANN, *Administrative Patent Judges*.

HAMANN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants file this appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1–21. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

THE CLAIMED INVENTION

Appellants' claimed invention relates to emulated electrically erasable ("EEE") memory systems. *See* Spec. ¶ 1. Claim 1 is illustrative of the subject matter of the appeal and is reproduced below.

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[1] According to Appellants, the real party in interest is Freescale Semiconductor, Inc. App. Br. 3.

1. A memory system, comprising:

a memory controller;

an address random access memory (RAM) coupled to the memory controller; and

a non-volatile memory (NVM) coupled to the memory controller;

wherein:

the non-volatile memory has an address portion and a data portion;

the address portion of the non-volatile memory provides data portion addresses and lookup addresses of valid data to the memory controller;

the memory controller loads the data portion addresses and stores them in the address RAM at locations defined by the lookup addresses of valid data; and

the memory controller uses the data portion addresses, and locations of the data portion addresses within the address RAM, to locate data blocks within the data portion of non-volatile memory.

REJECTIONS ON APPEAL

(1) The Examiner rejected claims 1–3, 16, and 19 under 35 U.S.C. § 102(b) as being anticipated by Lin et al. (US 2007/0106835 A1; published May 10, 2007) (hereinafter "Lin").

(2) The Examiner rejected claims 4–6, 9–12, 20, and 21 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lin and Li et al. (US 2010/0293320 A1; published Nov. 18, 2010) (hereinafter "Li").

(3) The Examiner rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lin, Li, and Chou et al. (US 2005/0120163 A1; published June 2, 2005) (hereinafter "Chou").

(4) The Examiner rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lin, Li, Chou, and Scouller et al. (US 2011/0107009 A1; published May 5, 2011) (hereinafter "Scouller").

(5) The Examiner rejected claims 17 and 18 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lin and Scouller.

(6) The Examiner rejected claims 13–15 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lin, Li, and Scouller.

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' contentions that the Examiner erred. In reaching our decision, we consider all evidence presented and all arguments made by Appellants.

We disagree with Appellants' arguments, and we incorporate herein and adopt as our own the findings, conclusions, and reasons set forth by the Examiner in (1) the November 20, 2014 Final Office Action ("Final Act." 2–13), (2) the February 24, 2015 Advisory Action ("Adv. Act." 2), and (3) the September 15, 2015 Examiner's Answer (Ans. 2–5). We highlight and address, however, specific findings and arguments below for emphasis.

(1) NVM has an address portion

Appellants argue Lin fails to disclose that "the non-volatile memory has an address portion," as recited in claim 1 and similarly recited in claim 16. App. Br. 11; Reply Br. 3–4. Specifically, Appellants contend Lin's NVM has no address portion — rather Lin's NVM only has a program code portion and a data portion. *Id.* (citing Lin ¶ 20).

The Examiner finds, and we agree, Lin discloses the disputed limitation. *See* Ans. 2–3; Final Act. 2–3. Specifically, the Examiner finds,

and we agree, Lin discloses "the associated data of [an] address translation table is also stored in a specific block of the data block of the flash memory," and thus, that portion of the flash memory (i.e., NVM) is an address portion in accordance with claim 1. Ans. 2 (citing Lin ¶ 31); Final Act. 2 (same).

(2) *Address portion provides data portion and lookup addresses*

Appellants argue Lin fails to disclose that "the address portion of the non-volatile memory provides data portion addresses and lookup addresses of valid data to the memory controller," as recited in claim 1 and similarly recited in claim 16. App. Br. 11; Reply Br. 3–4. Appellants argue Lin instead discloses "only the programming circuit and the MCU [("Micro Computer Unit")] 114 provide address and control signals to the memory controller." App. Br. 11–12 (citing Lin ¶ 21) (arguing "[t]he memory controller accesses the data in the NVM 312 through the first address/data signals A/D1 and the first control signals CS1 according to the second address/data signals A/D2 and the second control signals CS2" transferred from the MCU); Reply Br. 3 (citing Lin ¶¶ 21, 31) (arguing it is "the MCU in Lin [that] retrieves addresses from the embedded SRAM and provides addresses to the memory controller"); *see also* App. Br. 12 (citing Lin ¶ 31) (arguing Lin discloses the MCU stores the address translation table in SRAM).

Additionally, Appellants dismiss as inapposite the Examiner's findings regarding the addresses being provided indirectly — as opposed to directly — from the flash memory to the memory controller in Lin. *See* Reply Br. 3–4. Appellants argue regardless "the MCU only uses the address translation table in the non-volatile memory to recreate the address

translation table in the SRAM during reboot" and that information from the table in the NVM is never provided to the memory controller; only to the MCU. Reply Br. 4 (citing Lin ¶¶ 23, 31). Appellants further contend because "the memory controller of Lin does not perform address translation, it would not be necessary or desirable to pass the address translation table from the MCU to the memory controller in Lin." *Id.* (citing Lin ¶¶ 21–22); *see also id.* (arguing "neither the NVM or the MCU of Lin provide data portion addresses <u>and</u> lookup addresses of valid data to the memory controller").

The Examiner finds Lin discloses this disputed limitation. *See* Ans. 2–3; Final Act. 2–3. Specifically, the Examiner finds the "address table block also 'provides data portion addresses and lookup addresses of the valid data to the memory controller' because it can be used to create an address table in the SRAM which is used by the memory controller for address translation." Ans. 2 (citing Lin ¶ 31). The Examiner then finds these "addresses are provided [indirectly] via the SRAM rather than directly from the flash memory but ultimately the addresses are still provided from the flash memory *to* the memory controller." *Id.* at 2–3.

We agree with the Examiner that Lin discloses the disputed limitation. For example, we find Lin discloses that the address translation table (and its associated data) can be stored in the NVM so that the MCU can create a corresponding address translation table in SRAM. *See* Lin ¶ 31. Creating the table requires that the NVM provide the address translation table data to the memory controller which is an intermediate component located between (i) the MCU and NVM and (ii) the MCU and SRAM. *See* Lin Fig. 3, ¶ 31 (disclosing the memory controller reads and writes to the NVM). We also

agree with the Examiner that the memory controller also indirectly receives data portion addresses and lookup addresses from the NVM via the SRAM and/or MCU in accordance with the broadest reasonable interpretation of the claim language. *See id.*

(3) *Memory Controller*

Appellants argue Lin fails to disclose "a memory controller, coupled to the non-volatile memory and the processor, for receiving the system addresses and the data" and "the memory controller provides the look-up addresses to the address system and writes data into locations in the data portion selected by the look-up addresses," as recited in claim 16. App. Br. 12; Reply Br. 5. Specifically, Appellants argue Lin instead discloses:

> [T]he MCU 114 . . . provides address/data and control signals to the memory controller to allow the memory controller to access data in the NVM. The memory controller in Lin is not coupled to the NVM to receive the system addresses and the data as in claim 16; rather **the memory controller in Lin receives the system address and the data from the MCU**.

App. Br. 12 (emphasis added).

The Examiner finds Lin discloses the disputed limitations. *See* Final Act. 4. Specifically, the Examiner finds (i) Lin discloses the memory controller is coupled to the non-volatile memory and the processor, for receiving the system addresses and the data (*id.* (citing Lin Fig. 3; ¶¶ 19–21)) and (ii) "the memory controller provides the look-up addresses to the address system and writes data into locations in the data portion selected by the look-up addresses" (*id.* (citing Lin ¶ 31 (finding "the address for access is translated by the address translation table to access the corresponding block of the flash memory"))).

We are not persuaded of Examiner error. We find Lin discloses the memory controller is coupled to the non-volatile memory **and the processor**, for receiving the system addresses and the data. *See* Lin Fig. 3 (showing the memory controller 315 coupled to the MCU 114, the NVM 312, and the SRAM 113); ¶ 21. We note Appellants argue in the Appeal Brief that "the memory controller in Lin receives the system address and the data from the MCU," which is in accord with the claim language.

As to the latter disputed limitation, Appellants' Appeal Brief fails to sufficiently address why it is not disclosed by Lin. *See* 37 C.F.R. § 41.37(c)(1)(iv) (2012) ("A statement which merely points out what a claim recites will not be considered an argument for separate patentability of the claim."); *see also In re Lovin*, 652 F.3d 1349, 1357 (Fed. Cir. 2011) (holding that "the Board reasonably interpreted Rule 41.37 to require more substantive arguments in an appeal brief than a mere recitation of the claim elements and a naked assertion that the corresponding elements were not found in the prior art"). Appellants' Reply Brief makes a substantive attempt to address this latter disputed limitation, while also arguing in contradiction to the Appeal Brief that "the memory controller in Lin does not receive the system address from the MCU." Reply Br. 5 (citing Lin ¶ 31). However, Appellants have not shown good cause as to why this argument could not have been presented earlier. As such, this argument has not been considered, and is waived. *See Ex parte Borden*, 93 USPQ2d 1473, 1473–74 (BPAI 2010) (informative) (absent a showing of good cause, the Board is not required to address arguments in Reply Brief that could have been presented in the principal Appeal Brief).

(4) *Address RAM*

Appellants argue Lin fails to disclose "responsive to a system address provided by the processor, the address RAM provides, to the non-volatile memory, one of the data portion addresses from one of the locations in the address RAM selected by one of the lookup addresses," as recited in claim 2. App. Br. 13; Reply Br. 5. Appellants argue Lin instead discloses "that when the MCU want to access the data of the flash memory, the MCU reads the address of the data in the address translation table in the embedded SRAM, and then outputs the corresponding address bus signal and control signal to access the flash memory through the memory controller." App. Br. 13 (citing Lin ¶ 31). Appellants then assert "[t]his is different than claim 2, in which the address RAM provides the data portion address to the non-volatile (e.g., flash) memory instead of providing the address to the MCU as in Lin." *Id.*

The Examiner finds, and we agree, the claim language "does not require the RAM and the nonvolatile memory to be in direct communication with each other, only that an address is 'provided' from the RAM to the non-volatile memory." Ans. 3. The Examiner further finds, and we agree, "Lin discloses this limitation because the translated address bus signals and control signals are provided from the SRAM to the MCU (when the MCU reads the address translation table in the SRAM) and then from the MCU to the flash memory." *Id.* (citing Lin ¶ 31); *see also* Lin Fig. 3. The Examiner thus finds, and we agree, "the translated address signals are ultimately provided from the SRAM to the flash memory via the MCU." *Id.* Accordingly, we sustain the Examiner's rejection of claim 2.

(5) <u>*Logic gate*</u>

Appellants argue the combination of Lin and Li, and Li in particular, fails to teach or suggest "the system address further comprises the one of the data portion addresses, the memory system further comprising a logic gate that combines the one of the data portion addresses provided from the address RAM with the location in the data block to select valid data from the data portion, as recited in claim 4. *See* App. Br. 13. Specifically, Appellants argue Li instead teaches "a block address along with an offset address to identify data in a block, but Li does not disclose a logic gate that combines the block address and the offset address, or any logic gate that would combine any addresses in Lin." *Id.*

The Examiner finds that the combination teaches the disputed limitation. *See* Ans. 4; Final Act. 5. Specifically, the Examiner finds Li teaches "a memory block being addressed by a block address and an offset[, where t]he offset represents a 'location in the data block.'" Ans. 4 (citing Li Fig. 4; ¶¶ 71–74). The Examiner further finds "the term 'logic gate' used in the claim is broad and can refer to any logical circuit used in a computer system," including Li's "address translation table and memory block" which has logical processing "to allow the memory location to be addressed by the block and offset address." *See id.*; *see also* Final Act. 5.

We agree with the Examiner's findings that the combination, and Li in particular, teaches or suggests the disputed limitation. For example, we agree that the broadest reasonable interpretation in light of Appellants' Specification of "logic gate" includes any logical circuit. We also find that one of skill in the art would have found it obvious to employ the claimed logic gate to allow the memory location to be addressed by the block and

offset. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) ("[T]he [obviousness] analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.").

(6) *NVM location has first valid data and a lookup address*

Appellants argue the combination of Lin and Li fails to teach or suggest "identifying a first NVM location in the NVM, wherein the first NVM location has first valid data and a lookup address of the first valid data," as recited in claim 5. App. Br. 14; Reply Br. 6. Specifically, Appellants argue:

> [T]he NVM 312 of Lin has a program code portion and a data portion, but no lookup address of first valid data." (Lin, para. [0020]). Lin teaches that MCU 114 stores an address translation table in the embedded SRAM according to the number of writing times. (Lin, para. [0031]). To access data from the SRAM, the MCU reads the corresponding address of the address translation table from the embedded SRAM and then outputs the corresponding address bus signal and control signal to access the flash memory through the memory controller 315. (Id.)

App. Br. 14.

Appellants then argue "[t]he address table is stored in the memory controller 315 and an address translation table can be stored in the SRAM of Lin, but nothing in Lin teaches or suggests that the NVM includes a lookup address." *Id.*

The Examiner finds, and we agree, the broadest reasonable interpretation of "has . . . a lookup address of the valid data" includes "'has a lookup address associated with.'" Ans. 4. The Examiner further finds, and we agree, that "[t]he working region of the flash memory that stores data has

a lookup address associated with it that is stored in the address translation table." *Id.* (citing Lin ¶ 31). Thus, we find the combination teaches or suggests the disputed limitation.

(7) *Providing the address to the NVM from the address RAM*

Appellants argue the combination of Li and Lin, and Lin in particular, fails to teach or suggest "responsive to the system address for selecting the first RAM location, providing the address of the first NVM location to the NVM from the address RAM," as recited in claim 5. App. Br. 14; Reply Br. 6–7. Appellants argue Lin instead only teaches "the MCU stores the address translation table in the SRAM and reads the location of data in the SRAM to then provide and address and control signal to the SRAM." App. Br. 14 (citing Lin ¶ 31). Appellants also argue "the SRAM in Lin only includes a table that indicates the number of times the flash has been written." Reply Br. 7 (citing Lin ¶ 31). Appellants thus contend nothing "in Lin provides the address of the first NVM location to the NVM from the address RAM," in accordance with the claim language. App. Br. 14.

The Examiner finds, and we agree as above, the claim language does not require the address be provided directly from the RAM to the NVM. Ans. 5. The Examiner also finds, and we agree, "the MCU can read a corresponding translated address from the SRAM address translation table in order to access the flash memory." Ans. 5 (citing Lin ¶ 31). We find the translated address is provided from the SRAM, through the operations of the MCU and memory controller, to the NVM. *See* Lin Fig. 3; ¶ 31 (teaching, *inter alia*, the SRAM can contain an "address translation table" and associated data). Thus, we sustain the Examiner's rejection of claim 5.

CONCLUSION

Based on our findings above, we sustain the Examiner's rejections of claims 1, 2, 4, 5, and 16. We also sustain the Examiner's rejection of claims 3, 6–15, and 17–21 for which Appellants did not provide separate, substantive arguments for patentability.

DECISION

We affirm the Examiner's rejections of claims 1–21.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED