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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* JOHN R. NICKOLLS, BRETT W. COON, and  
MICHAEL C. SHEBANOW

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Appeal 2016-000874  
Application 12/888,409  
Technology Center 2100

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Before DEBRA K. STEPHENS, KEVIN C. TROCK, and  
JESSICA C. KAISER, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION ON APPEAL

*Introduction*

Appellants<sup>1</sup> appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1, 4–13, and 16–24. Claims 2, 3, 14, and 15 have been cancelled.

We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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<sup>1</sup> According to Appellants, the real party in interest is NVIDIA Corporation. (Final Act. 3).

### EXEMPLARY CLAIM

Claim 1, reproduced below, is illustrative of the claimed subject matter with disputed limitations emphasized:

1. A method for managing a parallel cache hierarchy in a processing unit, the method comprising:

receiving an instruction from a scheduler unit, wherein the instruction comprises a load instruction or a store instruction, and wherein the instruction is associated with an address that identifies a memory region;

determining that the instruction includes a cache operations modifier that identifies a policy for caching data associated with the instruction at one or more levels of the parallel cache hierarchy; and

executing the instruction and caching the data associated with the instruction based on the cache operations modifier, *wherein the data is cached if the address is in a local memory region, and the data is not cached if the address is in a global region.*

### REJECTIONS

The Examiner made the following rejections:

Claims 4–10 and 16–22 stand rejected under 35 U.S.C. § 112 first paragraph for lack of written description. (Final Act. 2–4).

Claims 1, 4–8, 11–13, 16–20, 23, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hass (US 2005/0055540 A1; published Mar. 10, 2005), Rosenbluth (US 2007/0079073 A1; published Apr. 5, 2007), and Hammarlund (US 2005/0138295 A1; published June 23, 2005). (Final Act. 4–8).

Claims 9, 10, 21, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hass, Rosenbluth, Hammarlund, and Boggs (US 6,877,086 B1; issued Apr. 5, 2005). (Final Act. 8–10).

## ISSUES

*Issue 1:* Did the Examiner err in finding Hass teaches “caching the data associated with the instruction based on the cache operations modifier, wherein the data is cached if the address is in a local memory region, and the data is not cached if the address is in a global region,” as recited in claim 1 and similarly recited in claim 13?

*Issue 2:* Did the Examiner err in finding claims 4–10 and 16–22 fail to comply with the written description requirement?

## ANALYSIS

### *Issue 1*

Appellants contend the Examiner erred in finding Hass teaches “caching the data associated with the instruction based on the cache operations modifier, wherein the data is cached if the address is in a local memory region, and the data is not cached if the address is in a global region,” as recited in claim 1 and similarly recited in claim 13. (App. Br. 11–14; Reply Br. 7–10). Specifically, Appellants argue Hass does not cache data based on whether “an address associated with the instruction is in a local memory region” or whether “the address is in a global memory region.” (Reply Br. 9 (emphasis omitted); App. Br. 12).

We are persuaded. The Examiner finds Hass teaches caching to a translation look-aside buffer (TLB), i.e., a cache, in two modes: partitioned mode and global mode. (Ans. 11; Final Act. 5). The Examiner further finds (Ans. 11) in partitioned mode only “an exclusive subset or portion of the main TLB” can be cached to and in global mode “any portion of the main TLB” can be cached to (Hass ¶ 82). While Hass teaches a partitioned mode,

in which certain partitions of a TLB are not cached to, and a global mode, in which any portion of the TLB can be cached to (Hass ¶ 82), the Examiner has not adequately explained how caching data in partitioned mode or global mode is based on local or global addresses as required by the claims (*see* Ans. 11–12; *see also* Final Act. 5, 10–11). Furthermore, the Examiner determines that “at the partitioned level of the TLB, if an address . . . does not belong to the owning thread, the data is not cached” and “global addresses are cached and viewed by all” (Ans. 11; Final Act. 10–11), but the Examiner’s cited portions of Hass do not discuss owning thread addresses or global addresses (*see* Hass ¶¶ 81–82, 84, 112) and the Examiner has not adequately explained which features of Hass teach such addresses. The Examiner does not rely on any other of the cited references to teach this limitation.

Accordingly, based on this record, we do not sustain the Examiner’s § 103 rejection of independent claims 1 and 13 and claims 4–12 and 16–24, which depend directly or indirectly from claims 1 and 13. The additional references, as applied by the Examiner in the rejections of independent claims 1 and 13 and dependent 4–12 and 16–24, do not cure the deficiency discussed above. Because we do not sustain the Examiner’s § 103 rejection of claims 1, 4–13, and 16–24 on this issue, we do not reach the merits of Appellants’ remaining § 103 arguments regarding those claims. (*See* App. Br. 13–14; Reply Br. 10–11).

#### *Issue 2*

While not necessary to our decision because we do not sustain the Examiner’s § 103 rejections, discussed *supra*, in the event of further prosecution, we address the Examiner’s § 112, first paragraph rejection of

claims 4–10 and 16–22 for failing to comply with the written description requirement.

Claim 4, which depends from claim 1, additionally recites “wherein the parallel cache hierarchy includes an L1 cache level and an L2 cache level.” As discussed above, claim 1 recites “data is cached if the address is in a local memory region, and the data is not cached if the address is in a global region.” Claim 16, which depends from independent claim 13, recites similar limitations. The Examiner finds that the rejected “claim[s] require[ ] the data to be cached or not cached,” but Appellants’ Specification only discloses that “data is cached in L1 and L2 or only cached in L2.” (Ans. 10 (emphasis omitted); *see* Final Act. 3–4). That is, the Examiner finds the Specification discloses caching or not caching data to a particular cache (L1), but does not disclose caching or not caching data at all.

Appellants contend the Examiner erred in determining claims 4–10 and 16–22 fail to comply with the written description requirement. (App. Br. 10–11; Reply Br. 5–7). Specifically, Appellants argue the claimed “L1 cache level” and “L2 cache level” are disclosed in Figures 5–7 and paragraphs 66, 67, and 77–119 of Appellants’ Specification. (App. Br. 10; Reply Br. 5). Appellants further argue caching data “based on the cache operations modifier, wherein the data is cached if the address is in a local memory region, and the data is not cached if the address is in a global region,” as recited in the claims, is disclosed by the Table 1 of the Specification, which discloses when “the memory address associated with the load instruction is a local address, then the data is cached in L1 (i.e., evict-first)” and when “the memory address associated with the load instruction is a global address, then the data is not cached in L1 (i.e., non-

cached).” (Reply Br. 5 (emphasis omitted) (citing Spec. Table 1, ¶¶ 84, 93, 118, Figs. 6–7); App. Br. 10–11 (citing Spec. ¶ 117)).

We are persuaded by Appellants’ arguments. Appellants’ Specification discloses caching or not caching data because data is cached or not cached to cache L1. In particular, Appellants’ Specification teaches a load instruction with cache operation “.cd” which instructs the system to cache to L1 for local addresses and to not cache to L1 for global addresses. (Spec. Table 1, ¶¶ 76–77, 84). Accordingly, we are persuaded claims 4–10 and 16–22 comply with the written description requirement of 35 U.S.C § 112, first paragraph.

#### DECISION

For the above reasons, the Examiner’s rejections of claims 1, 4–13, and 16–24 are reversed.

REVERSED