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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte AVIGDOR SEGAL, IGAL MALY, BORIS BARSKY, and
ILAN BAR

Appeal 2016-000434
Application No. 13/070,245¹
Technology Center 2100

Before MARC S. HOFF, NORMAN H. BEAMER, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1–18 and 21, which constitute all the claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' invention is a system and method for storing data to non-volatile memory that has a portion operating as a multi-level cell (MLC) memory that stores data in pages, and a portion operating as a single-level cell (SLC) memory. An instruction is received to write a dataset to said non-

¹ The real party in interest is Densbits Technologies Ltd.

volatile memory. If the size of the dataset is equal to the size of an integer number of pages, the dataset may be written directly to the MLC portion. If the size of the dataset is different than the size of an integer number of pages, at least a portion of the dataset may be written temporarily to the SLC memory portion, until data is accumulated in a plurality of write operations to the SLC memory portion having a size equal to the size of an integer number of pages. *See Spec. ¶ 6.*

CLAIMED SUBJECT MATTER

Claim 1 is exemplary of the claims on appeal:

1. A device comprising:

a non-volatile memory including a portion operating as a multi-level cell memory storing data in pages and a portion operating as a single-level cell memory electrically connected to the multi-level cell memory portion; and

a processor to receive an instruction to write a dataset to the non-volatile memory,

wherein if the size of the dataset is equal to the size of an integer number of the pages,

the processor writes the dataset directly to the multi-level cell memory portion to fill the integer number of the pages in the multi-level cell memory portion in a single write operation; and

wherein if the size of the dataset is larger than the size of the integer number of the pages, the processor writes a portion of the dataset equal to the integer number of the pages directly to the multi-level cell memory portion and a remaining portion of the dataset smaller than the size of the page to the single-level cell memory portion;

wherein when data is accumulated in a plurality of write operations to the single-level cell memory portion having a size equal the size of a page the processor writes the accumulated data from the single-level cell memory portion to fill a in the multi-level cell memory portion in a single write operation.

REFERENCES

The Examiner relies upon the following prior art in rejecting the claims on appeal:

KIM	US 2008/0159012 A1	July 3, 2008
LY	US 2008/0183949 A1	July 31, 2008
YU	US 2008/0209112 A1	Aug. 28, 2008
CHEN	US 2009/0204746 A1	Aug. 13, 2009
LEE	US 2009/0248965 A1	Oct. 1, 2009
RADKE	US 2009/0248952 A1	Oct. 1, 2009
JANSSEUNE	US 2010/0175053 A1	July 8, 2010
SPROUSE	US 2011/0153911 A1	June 23, 2011

REJECTIONS ON APPEAL

Claims 1, 2, 7, 10–13, 18, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, Radke, Sprouse, Chen, and Jansseune.

Claims 3 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, Radke, Sprouse, Chen, Jansseune, and Ly.

Claims 4–6 and 15–17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, Radke, Sprouse, Chen, Jansseune, and Yu.

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, Radke, Sprouse, Chen, Jansseune, and Kim.

Throughout this decision, we make reference to the Appeal Brief (“App. Br.,” filed Dec. 1, 2014) and the Examiner’s Answer (“Ans.,” mailed Aug. 7, 2015) for their respective details.

ISSUE

Does the combination of Lee, Radke, Sprouse, Chen, and Jansseune teach or suggest writing a portion of a dataset equal to an integer number of memory data pages directly to a multi-level cell memory portion, and writing a remaining portion of said dataset, smaller than the size of such a memory data page, to a single-level cell memory portion?

PRINCIPLES OF LAW

To teach away, prior art must “criticize, discredit, or otherwise discourage the solution claimed.” Mere disclosure of alternative embodiments is not a teaching away. *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004).

ANALYSIS

CLAIMS 1, 2, 7, 10–13, 18, AND 21

We do not agree with Appellants that Lee teaches away from the claimed invention. *See* App. Br. 9. The Examiner cites Lee for its teaching that if the size of the dataset is equal to the size of an integer number of pages, the processor writes the dataset directly to the multi-level cell memory portion to fill an integer number of pages in the MLC in a single write operation. Ans. 3, citing Lee ¶ 55. Appellants do not contest this. Lee also teaches that “when the data size is not greater than the predetermined data size,” “the data are written in log block of the SLC flash memories.” Lee ¶ 55. Appellants do not point to any teaching in Lee that criticizes, discredits, or discourages the solution claimed in the application under appeal. *See Fulton*, 391 F.3d at 1201. Appellants have therefore failed to establish that Lee contains any teaching away from the invention claimed.

We do not agree with Appellants that Chen teaches away from the claimed invention. *See* App. Br. 10. Similar to Lee, Chen teaches that

if the size of the file exceeds a predetermined value, the control unit 52 sets the channel 62 to link to the MLC NAND flash memory 54, and then stores the file in the MLC NAND flash memory Otherwise, the control unit sets the channel to link to the SLC NAND flash memory 56, and then stores the file in the SLC NAND flash memory.

¶ 22. As in the case of Lee, Appellants have not cited to any portion of Chen that criticizes, discredits, or discourages Appellants’ claimed approach. *See Fulton*, 391 F.3d at 1201. Appellants have therefore failed to establish that Chen teaches away from the invention claimed.

We are not persuaded by Appellants’ argument that Jansseune does not teach or suggest storing a remaining portion of the dataset after a portion of the dataset equal to the integer number of pages was directly written to the multi-level cell memory portion. *See* App. Br. 11. Lee, rather than Jansseune, is relied upon for a teaching of a dataset equal to an integer number of pages being written to the MLC memory portion. *See* Ans. 3. The Examiner relies on Jansseune for its teaching that an amount of data that is smaller than the size of a memory “page” is written to a “common memory space” such as a single-level cell memory portion. Ans. 4, citing Jansseune ¶¶ 68, 78.

We do not agree with Appellants that Jansseune teaches away from the claimed invention. *See* App. Br. 11. Appellants correctly summarize Jansseune’s stated purpose for the grouping done by the grouping unit, i.e. “to minimize the copy load” and store the software items in a single On-Demand Paging (ODP) page. *See* App. Br. 11–12; Jansseune ¶ 68. Appellants do not identify any teaching in Jansseune that criticizes,

discredits, or discourages Appellants' approach. *See Fulton*, 391 F.3d at 1201. Appellants have therefore failed to establish that Jansseune teaches away from the invention claimed.

We find that the Examiner did not err in rejecting claims 1, 2, 7, 10–13, 18, and 21 as being unpatentable over Lee, Radke, Sprouse, Chen, and Jansseune. We sustain the Examiner's § 103 rejection.

CLAIMS 3 AND 14

As noted *supra*, we do not agree that Lee teaches away from the invention recited in claim 1, from which claim 3 depends. Appellants repeat the claim 1 argument that Lee writes the entire data to a multi-level cell memory. *See* App. Br. 13. However, as Appellants have not identified any portion of Lee that criticizes, discredits, or discourages Appellants' approach, Appellants have failed to establish that Lee teaches away from the invention recited in claim 3.

We also do not agree with Appellants that Ly teaches away from the claimed invention. *See* App. Br. 13. The Examiner relies on Ly to teach that a partial page block may be assigned and filled with data until a page is filled. Ans. 7; Ly ¶¶ 12, 15. Appellants' allegation that Ly discusses "writing data only to one type of memory" (App. Br. 13) does not equate to Ly criticizing, discrediting, or discouraging the approach taken by Appellants. *See Fulton*, 391 F.3d at 1201. We conclude that Ly does not teach away from the invention under appeal.

We find that the Examiner did not err in rejecting claims 3 and 14 as being unpatentable over Lee, Radke, Sprouse, Chen, Jansseune, and Ly. We sustain the Examiner's § 103 rejection.

CLAIMS 4–6 AND 15–17

Appellants do not discuss these claims in the Brief. Accordingly, we sustain *pro forma* the rejection of claims 4–6 and 15–17 under 35 U.S.C. § 103(a) as being unpatentable over Lee, Radke, Sprouse, Chen, Jansseune, and Yu.

CLAIMS 8 AND 9

Appellants do not discuss these claims in the Brief. Accordingly, we sustain *pro forma* the rejection of claims 8 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Lee, Radke, Sprouse, Chen, Jansseune, and Kim.

CONCLUSION

The combination of Lee, Radke, Sprouse, Chen, and Jansseune teaches writing a portion of a dataset equal to an integer number of memory data pages directly to a multi-level cell memory portion, and writing a remaining portion of said dataset, smaller than the size of such a memory data page, to a single-level cell memory portion.

DECISION

The Examiner's decision to reject claims 1–18 and 21 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED