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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/239,133	09/21/2011	Reza Shahidi	102304US	1087

15055 7590 11/18/2016
Patterson & Sheridan, L.L.P.
Qualcomm
24 Greenway Plaza, Suite 1600
Houston, TX 77046

EXAMINER
PHUNKULH, BOB A

ART UNIT	PAPER NUMBER
2412	

NOTIFICATION DATE	DELIVERY MODE
11/18/2016	ELECTRONIC

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ocpat_uspto@qualcomm.com

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte REZA SHAHIDI, JON J. ANDERSON, and ERIC S. MATTIS[1]

Appeal 2015-007645
Application 13/239,133
Technology Center 2400

Before ALLEN R. MacDONALD, BRUCE R. WINSOR, and PHILLIP A. BENNETT, *Administrative Patent Judges*.

BENNETT, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1, 3–14, 16–21, 23–25, 27–38, 40–45, 47–49, 51–62, 64–69, 71–73, 75–86, 88–93, 95, and 96.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE, and enter A NEW GROUND OF REJECTION.

---

[1] Appellants' Brief ("App. Br.") identifies QUALCOMM, Incorporated, San Diego, California as the real party in interest. App. Br. 4.

[2] Claims 15, 22, 39, 46, 63, 70, 87, and 94 are objected to as depending from a rejected base claim, and not at issue in this appeal.

CLAIMED SUBJECT MATTER

The claims are directed to touch temperature management based on power dissipation history. *See* Spec. ¶ 3. Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A method for wireless communications, comprising:
>
> monitoring estimated one or more powers dissipated by one or more parts of an apparatus over a period of time;
>
> monitoring one or more temperatures of the one or more parts; and
>
> adjusting at least one Quality of Service (QOS) aspect of the apparatus based on the monitored estimated one or more powers and monitored one or more temperatures of the one or more parts.

App. Br. 15 (Claims Appendix). The pending claims include four independent claims—claims 1, 25, 49, and 73—each of which is of generally similar scope.

REJECTIONS

Claims 1, 3–6, 11–14, 16, 21, 23, 25, 27–30, 35–38, 40, 45, 47, 49, 51–54, 59–62, 64, 69, 71, 73, 75–78, 83–86, 88, 93, and 95[3] stand rejected under 35 U.S.C. § 102(b) as being anticipated by Raith (US 6,760,311 B1, issued July 6, 2004).

Claims 7, 8, 31, 32, 55, 56, 79, and 80 stand rejected under 35 U.S.C. § 103(a) as being obvious over Raith.

---

[3] We note that the Final Office Action ("Final Act.") includes claims 2, 26, 50, and 74 in the rejection under 35 U.S.C. § 102(b). Final Act. 2. These claims were previously cancelled, and they are not at issue here.

Claims 9, 10, 24, 33, 34, 48, 57, 58, 72, 81, 82, and 96 stand rejected under 35 U.S.C. § 103(a) as being obvious over Raith and Aleksic et al. (US 2008/0057894 A1, published Mar. 6, 2008).

Claims 17–20, 41–44, 65–68, and 89–92 stand rejected under 35 U.S.C. § 103(a) as being obvious over Raith and Funk (US 6,169,884 B1, issued Jan. 2, 2001).

ISSUES FOR DECISION

(1) Does Raith disclose the limitation of "monitoring estimated one or more powers dissipated by one or more parts of an apparatus over a period of time" recited in independent claim 1?

(2) Does Raith disclose the limitation of "the adjusting is performed based on a known function between the estimated one or more powers, a duration of time, and a surface temperature of the apparatus" as recited in dependent claim 4?

(3) Does Raith disclose the limitation of "the threshold level is based on an ambient temperature associated with the apparatus" as recited in claim 6?

ANALYSIS

First Issue—Claim 1

In rejecting claim 1, the Examiner finds that Raith discloses "monitoring estimated one or more powers dissipated by one or more parts of an apparatus over a period of time." Final Act. 3 (citing Raith, col. 2, ll. 27–42); Ans. 2–3 (citing Raith, Abstract, col. 1, ll. 48–59, col. 9, ll. 31–36). More particularly, the Examiner finds that Raith discloses measuring operating temperature of the power amplifier, and operating temperature is

directly related to power dissipation. Ans. 11. According to the Examiner, measuring heat dissipation or temperature of the power amplifier is the same as measuring power dissipation of one or more parts of Raith's mobile phone. *Id.*

Appellants dispute the Examiner's findings. App. Br. 9–10; Reply Br. 2–3. Appellants argue that Raith is silent with respect to monitoring estimated power dissipation. App. Br. 9; Reply Br. 2. Appellants further argue that merely measuring an operating temperature is not the same as "monitoring estimated one or more powers dissipated by one or more parts" because power dissipation is not the only factor that contributes an operating temperature. App. Br. 9–10; Reply Br. 2. According to Appellants, ambient temperature and thermal conductivity may also contribute to power dissipation, and a device cannot monitor estimated power dissipation based solely on a measured operating temperature. App. Br. 9–10; Reply Br. 2–3.

We agree with Appellants that the Examiner has failed to show that Raith discloses "monitoring estimated one or more powers dissipated by one or more parts of an apparatus over a period of time." The passages in Raith cited by the Examiner describe a mobile device in which temperature measurements of a power amplifier are taken and provided to the processor. When the temperature measurement exceeds a predetermined threshold temperature, the mobile device reduces its transmission rate in order to lower its temperature. Raith, col. 1, ll. 25–39. Although Raith teaches as a general matter that "roughly half of the generated power is lost which in the form of heat dissipation in the power amplifier" (*id.* at col. 1, ll. 52–53), this general knowledge is not the same as "monitoring estimated one or more powers dissipated by one or more parts" at least because no power

dissipation value is computed or expressed. We further note that because Raith does not disclose "monitoring estimated one or more powers dissipated by one or more parts of an apparatus over a period of time," it also cannot disclose "adjusting at least one Quality of Service (QOS) aspect of the apparatus based on the monitored estimated one or more powers" as recited in claim 1 (emphasis added). Accordingly, we do not sustain the rejections of (1) claim 1; (2) independent claims 25, 49, and 73, which recite limitations substantially similar to those we find to not be disclosed by Raith and were rejected on substantially the same bases as claim 1; and (3) claims 3–14, 16–21, 23, 24, 27–38, 40–45, 47, 48, 51–62, 64–69, 71, 72, 75–86, 88–93, 95, and 96, which variously depend from claims 1, 25, 49, and 73.

Second Issue—Claim 4

Claim 4 depends from claim 1, and recites the additional limitation "the adjusting is performed based on a known function between the estimated one or more powers, a duration of time, and a surface temperature of the apparatus." App. Br. 15 (Claims Appendix). The Examiner finds this limitation disclosed in Raith because Raith discloses adjusting the transmission rate based on a comparison of the measured temperature with a known temperature threshold. Ans. 4 (citing Raith, col. 2, ll. 28–42, col. 4, ll. 25–39).

Appellants argue that the comparison of the measured temperature to the temperature threshold is not a function based on three different variables as required by claim 4. App. Br. 10–11; Reply Br. 3. Appellants further contend that Raith is entirely devoid of any disclosure of a "surface temperature" of an apparatus. App. Br. 11; Reply Br. 3.

We agree with Appellants. The Examiner points to nothing in Raith that indicates that the surface temperature of the apparatus is measured. The Examiner's reliance on Raith's teaching of measuring the heat within the housing of the mobile device is insufficient because the inside of the mobile device is not the surface of the mobile device. Thus, the Examiner has not shown by a preponderance of evidence that Raith teaches the limitation recited in claim 4, and for this additional reason we do not sustain the Examiner's rejection of claim 4 and claims 28, 52, and 76, which recite substantially the same limitations.

Third Issue—Claim 6

Claim 6 also depends from claim 1, and includes the further limitation "wherein the threshold level is based on an ambient temperature associated with the apparatus." App. Br. 15 (Claims Appendix). The Examiner finds that this limitation is met by the disclosure in Raith of the temperature being pre-programmed based on the capabilities of the mobile device and stored in the memory 180 of the mobile device and the threshold temperature being set to indicate whether or not the mobile station is overheating. Ans. 13 (citing Raith, col. 4, ll. 40–51, col. 7, ll. 45–60).

Appellants argue, and we agree, that Raith fails to teach the threshold temperature is based on an ambient temperature. App. Br. 11. We further agree with Appellants' contention that Raith does not discuss with any specificity the basis for determining the threshold temperature. *Id.* Accordingly, for this additional reason, we do not sustain the rejection of claim 6 and claims 30, 54, and 78, which recite substantially the same limitations.

NEW GROUND OF REJECTION—35 U.S.C. § 103(a)

Claims 1, 25, 49, and 73are newly rejected under 35 U.S.C. § 103(a) as being obvious over Raith and Gumma et al. (US 2007/0157035 A1, published July 5, 2007) ("Gumma").[4]

We adopt the Examiner's findings with respect to claim 1 (and the other independent claims) as set forth in the Final Office Action with the exception of the erroneous findings that Raith discloses "monitoring estimated one or more powers dissipated by one or more parts of an apparatus over a period of time" and "adjusting at least one Quality of Service (QOS) aspect of the apparatus based on the monitored estimated one or more powers" which were discussed *supra*. We also adopt the Examiner's findings with respect to the dependent claims.

Although Raith does not disclose "monitoring estimated one or more powers dissipated by one or more parts of an apparatus over a period of time" and "adjusting at least one Quality of Service (QOS) aspect of the apparatus based on the monitored estimated one or more powers," we find Gumma, in the same field of endeavor, teaches these limitations.

Gumma teaches, in the context of mobile computing platforms, estimating dynamic power consumption of semiconductor devices such as microprocessors. Gumma ¶¶ 8–10. Thus, Gumma teaches "monitoring estimated one or more powers dissipated by one or more parts of an apparatus." Moreover, Gumma teaches that this monitoring can be

[4] To ensure the record is clear, we note that this new ground does not obviate our findings regarding claims 4 and 6 and corresponding claims 28, 30, 52, 54, 76, and 78 which were discussed above.

performed "over a period of time." Specifically, Gumma states that "[t]he device power estimate may be calculated over a predetermined time period by adding the number of sentinel node assertions during that time period." Gumma ¶ 20. As such, the disclosure in paragraphs 8–10 of Gumma teaches the limitation "monitoring estimated one or more powers dissipated by one or more parts of an apparatus over a period of time" as recited in claim 1, and similarly recited in claims 25, 49, and 73.

Gumma also discloses, teaches, and otherwise suggests "adjusting at least one Quality of Service (QOS) aspect of the apparatus based on the monitored estimated one or more powers." Gumma, Fig. 3 (block 308), ¶ 39. Specifically, Gumma teaches that "[i]f the power estimate exceeds a predetermined threshold, and/or if the calculated temperature exceeds a predetermined threshold, all or portions of the device may be throttled." Gumma ¶ 39.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Raith and Gumma because they both are directed to addressing similar issues of heat and power management in mobile devices. Moreover, Gumma recognizes that "[r]untime power estimates may enhance the ability of dynamic power management techniques to evaluate power-performance tradeoffs and may deliver improved system performance." Gumma ¶ 2. Gumma further teaches using power estimates to predict the temperature of the device, and using the power estimates and/or temperature predictions to throttle device activity. Gumma ¶¶ 23, 26, Fig. 3 (block 308). As noted above, Raith teaches using direct temperature measurements to reduce, i.e., throttle, transmission rates. Raith, col. 4, ll. 25–39. A person of ordinary skill in the

art would have been motivated to use Raith's direct temperature measurements in the place of Gumma's temperature predictions in order to have more accurate temperature data that is independent of the power estimates.

Dependent Claims

We have entered new grounds of rejection for independent claims 1, 25, 49, and 73. We leave to the Examiner to consider the patentability of dependent claims 3, 5, 7–14, 16–21, 23–25, 27, 29, 31–38, 40–45, 47–49, 51, 53, 55–62, 64–69, 71–73, 75, 77, 79–86, 88–93, 95, and 96 in light of our findings and conclusions *supra*, regarding the independent claims. *The fact that we did not enter new grounds of rejection for the dependent claims should not be construed to mean that we consider the identified dependent claims to be patentable over the prior art of record.*

DECISION

The Examiner's rejection of claims 1, 3–6, 11–14, 16, 21, 23, 25, 27–30, 35–38, 40, 45, 47, 49, 51–54, 59–62, 64, 69, 71, 73, 75–78, 83–86, 88, 93, and 95 under 35 U.S.C. § 102(b) is reversed.

The Examiner's rejection of claims 7, 8, 31, 32, 55, 56, 79, and 80 under 35 U.S.C. § 103(a) as being obvious over Raith is reversed.

The Examiner's rejection of claims 9, 10, 24, 33, 34, 48, 57, 58, 72, 81, 82, and 96 under 35 U.S.C. § 103(a) as being obvious over Raith and Aleksic is reversed.

The Examiner's rejection of claims 17–20, 41–44, 65–68, and 89–92 under 35 U.S.C. § 103(a) as being obvious over Raith and Funk is reversed.

Claims 1, 25, 49, and 73are newly rejected under 35 U.S.C. § 103(a) as being obvious over Raith and Gumma.

NEW GROUND OF REJECTION

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b). Section 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review." Section 41.50(b) also provides:

> When the Board enters such a non-final decision, the appellant, within two months from the date of the decision, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:
>
> (1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new Evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the prosecution will be remanded to the examiner. The new ground of rejection is binding upon the examiner unless an amendment or new Evidence not previously of Record is made which, in the opinion of the examiner, overcomes the new ground of rejection designated in the decision. Should the examiner reject the claims, appellant may again appeal to the Board pursuant to this subpart.
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same Record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

Further guidance on responding to a new ground of rejection can be found in the Manual of Patent Examining Procedure § 1214.01.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED
37 C.F.R. § 41.50(b)

Notice of References Cited	Application/Control No. 13/239,133	Applicant(s)/Patent Under Patent Appeal No. SHAHIDI ET AL.	
	Examiner Bob Phunkulh	Art Unit 2400	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2007/0157035 A1	07-2007	Gumma et al.	713/300
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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(19) United States

(12) Patent Application Publication

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(43) Pub. Date: Jul. 5, 2007

Gumma et al.

(54) METHOD, SYSTEM, AND APPARATUS FOR RUNTIME POWER ESTIMATION

(75) Inventors: **Madhu Gumma**, Austin, TX (US); **Anand Ramachandran**, Austin, TX (US); **Eric Samson**, Folsom, CA (US)

Correspondence Address:
INTEL CORPORATION
c/o INTELLEVATE, LLC
P.O. BOX 52050
MINNEAPOLIS, MN 55402 (US)

(73) Assignee: **Intel Corporation**

(21) Appl. No.: **11/323,136**

(22) Filed: **Dec. 29, 2005**

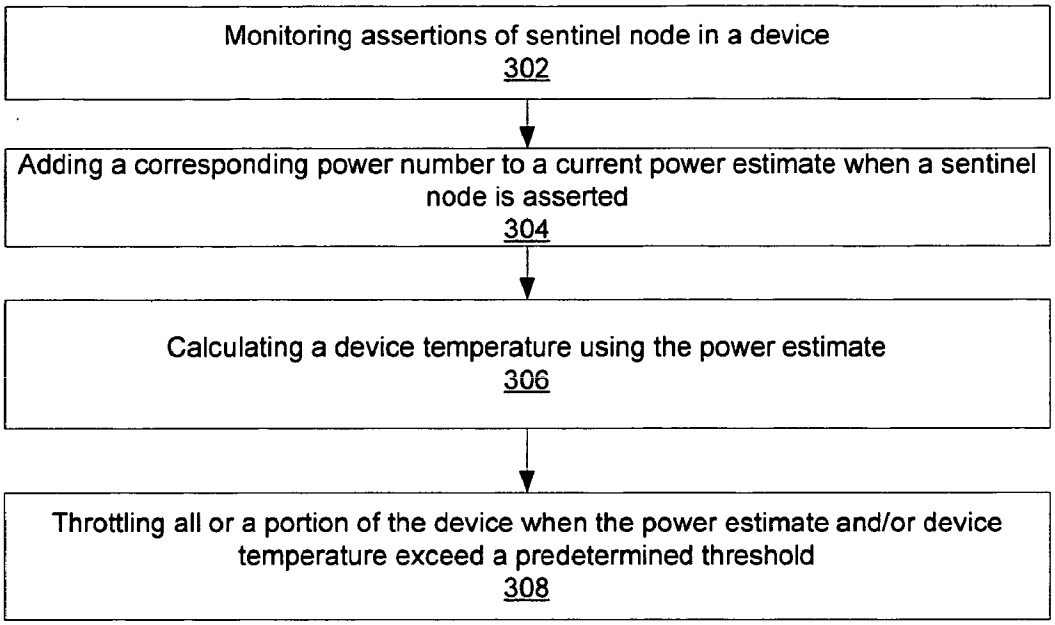
Publication Classification

(51) **Int. Cl.**
G06F 1/00 (2006.01)

(52) **U.S. Cl.** **713/300**

(57) **ABSTRACT**

Assertions of sentinel nodes within a device may be used to calculate device power consumption at runtime. These power estimates may be used to estimate a device temperature or leakage power, and/or may be used to make device throttling decisions.



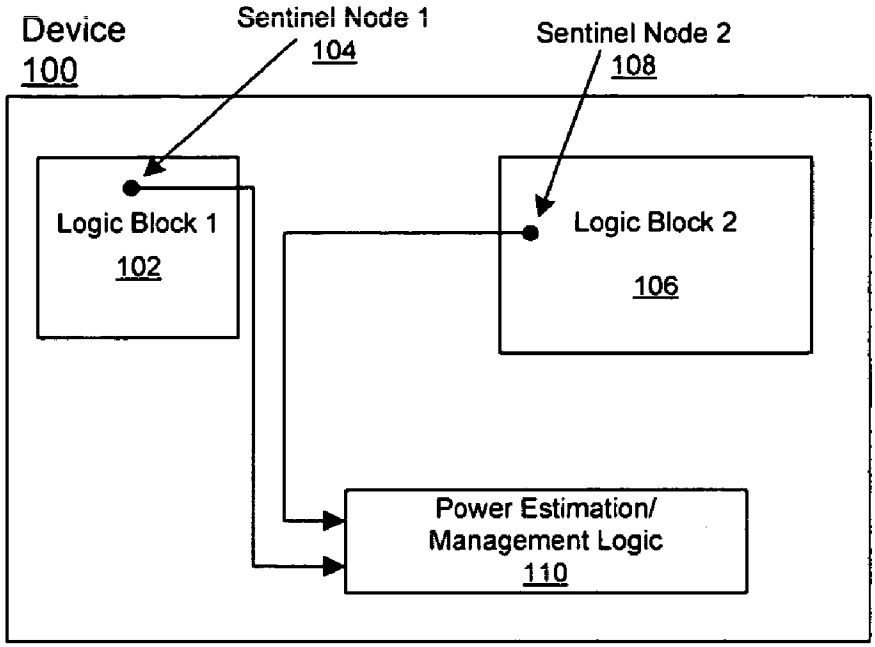

Device
100
Sentinel Node 1
104
Sentinel Node 2
108
Logic Block 1
102
Logic Block 2
106
Power Estimation/
Management Logic
110

FIG. 1

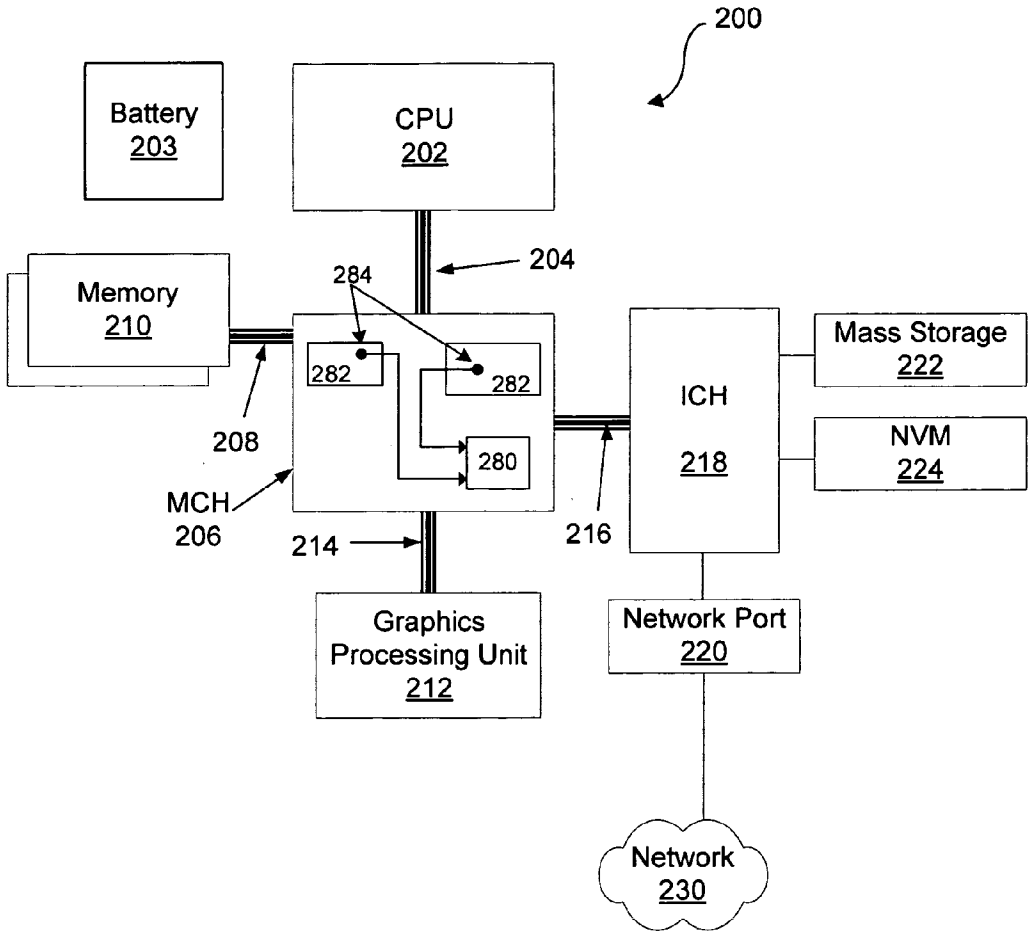

200
Battery
203
CPU
202
204
Memory
210
284
282
282
280
208
MCH
206
214
216
ICH
218
Mass Storage
222
NVM
224
Graphics
Processing Unit
212
Network Port
220
Network
230

FIG. 2

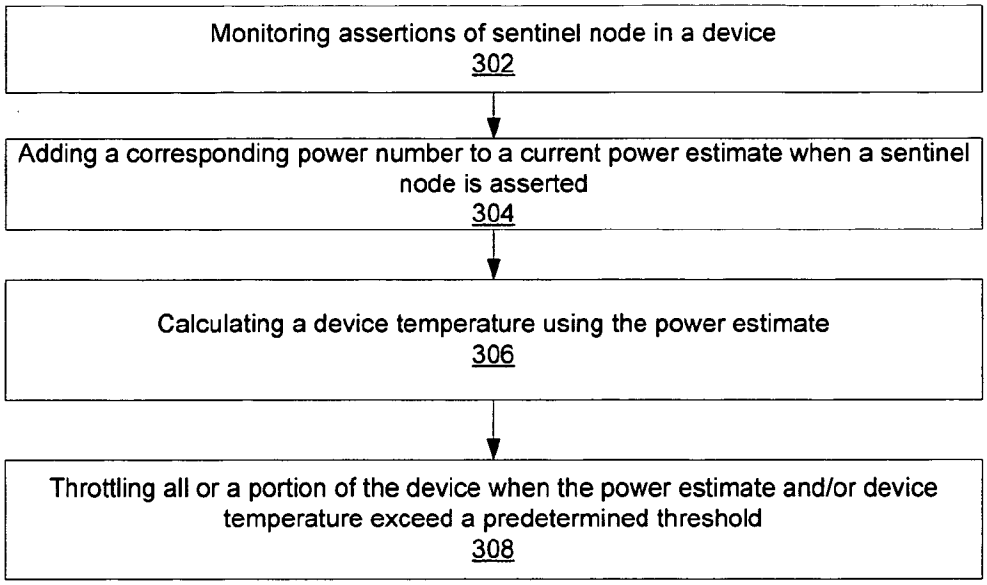

Monitoring assertions of sentinel node in a device
302
Adding a corresponding power number to a current power estimate when a sentinel node is asserted
304
Calculating a device temperature using the power estimate
306
Throttling all or a portion of the device when the power estimate and/or device temperature exceed a predetermined threshold
308

FIG. 3

METHOD, SYSTEM, AND APPARATUS FOR RUNTIME POWER ESTIMATION

BACKGROUND

[0001] Embodiments of the present invention relate to power management techniques for computing devices and more specifically to estimation of dynamic power consumption of a device at runtime.

[0002] As electronic devices continue to become smaller in size and higher performance, heat removal and power density of semiconductor devices become increasingly challenging. The ability to measure the power dissipation of a chip at runtime may enable temperature-and reliability-aware computing. Runtime power estimates may enhance the ability of dynamic power management techniques to evaluate power-performance tradeoffs and may deliver improved system performance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] An understanding of embodiments of the present invention may be obtained from the following detailed description in conjunction with the following drawings, in which:

[0004] FIG. **1** is an illustration of a device implementation of sentinel nodes according to some embodiments.

[0005] FIG. **2** is an illustration of a system block diagram according to some embodiments.

[0006] FIG. **3** is a flow diagram according to some embodiments.

DETAILED DESCRIPTION

[0007] In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of embodiments of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention as hereinafter claimed.

[0008] Embodiments of the present invention concern estimation of the dynamic power consumption of a semiconductor device at runtime. Although the following discussion centers on semiconductor devices commonly used in mobile computing platforms, such as memory controller devices, input/output controller devices, graphics controllers, and microprocessors, it will be understood by those skilled in the art that embodiments of the present invention as hereinafter claimed may be practiced in support of any type of semiconductor device.

[0009] In some embodiments, dynamic power consumption (P_{dyn}) of a circuit may be calculated using the following equation:

$$P_{dyn}=C*V^2*f*a$$

[0010] Where, C is the capacitance of the circuit, V is the supply voltage, f is the circuit clock frequency, and a is an activity or switching factor. Because the capacitance (C), supply voltage (V) and frequency (f) are fixed quantities, it is possible to estimate the dynamic power consumption of a device at runtime by estimating the activity factor of the device (a) at runtime. The activity factor is an indication of the amount of work done in a logic circuit and may be determined by the switching activity of the circuit.

[0011] For a chip or device, the total power consumption is equal to the sum of power consumed by each logic block within the device. A logic block may be an entire device, or a logic block may define a smaller portion within the device. For example, a logic block may encompass a front side bus interface or a memory controller interface. In other embodiments, a logic block may encompass only the read portion or write portion of such an interface. In yet other embodiments, a logic block may include as few as one gate or signal, or may include only a few gates or signals. Thus, a chip or device may be comprised of one or more logic blocks.

[0012] The total power consumption for a chip or device may be computed by summing the power of each logic block within the device as follows:

$$P_{chip}=P_{LogicBlock1}+\ldots+P_{LogicBlockN}$$

Thus, $P_{chip}=(C*V^2*f*a)_{LogicBlock1}+\ldots+(C*V^2*f*a)_{LogicBlockN}$

[0013] $C*V^2*f$ is a constant value for each logic block. In this equation, only the activity factor, a, changes depending on the activity of each logic block. Thus, the total power of the device, P_{chip}, may be computed using the following equation:

$$P_{chip}=(W_1*A_1)+\ldots+(W_N*A_N)$$

[0014] Here, W_i is a constant, weighted value representing $C*V^2*f$ for logic block i. A_i is equal to the number of assertions of a sentinel signal or sentinel node representing logic block i, and A_i is proportional to the architectural activity of logic block i. A sentinel node is a signal in a logic block whose activity is representative of the architectural activity of the entire logic block. A sentinel node toggles (e.g. is asserted or de-asserted) whenever its associated architectural event occurs. An architectural event may be, but is not limited to, an event such as a read, write, a logic operation (e.g. add), or other event in the device which causes total power to increase. For the purposes of this disclosure, an assertion, de-assertion, toggle, and/or state change of the sentinel node may all serve the purpose of indicating architectural activity within a logic block, and are thus hereinafter referred to as "assertions" of the sentinel node.

[0015] The weighted value, W_i, for each block may be calculated by simulating a device with test inputs and measuring power consumption. By performing a linear regression analysis on the P_{chip} equation above, a weight W_i may be obtained for each logic block in the chip. Each logic block may have a different weighted value, W_i. For example, if approximately the same amount of architectural activity as indicated by sentinel node assertions occurs in each of two logic blocks, but the first logic block includes more gates and/or consumes more power, then the weighted value for the first logic block may be greater than the weighted value for the second logic block.

[0016] Thus, the total average device power may be calculated by adding a logic block's weighted value, W_i, to a total average power value each time a sentinel node in the block is asserted. Therefore, by monitoring a selected set of signals that reflect the activity of the logic blocks they represent, the power consumption for a device may be estimated.

[0017] FIG. 1 illustrates sentinel nodes that may be used to measure architectural activity in a device according to some embodiments. A device or chip (100) may include one or more logic blocks (102,106), and each logic block may include one or more sentinel nodes (104,108). Device (100) may be any type of device for which it is desirable to compute runtime power estimations, including, but not limited to, processors, chipset devices, memory devices, graphics devices, application specific integrated circuits (ASICS) or any other type of electronic component.

[0018] Each logic block includes one or more sentinel nodes (104,108). A sentinel node may be selected so as to reflect the activity of the corresponding logic block it represents. For example, sentinel node 104 is selected such that its activity is a representation of the overall architectural activity of logic block 102.

[0019] The sentinel nodes in each logic block may be monitored by power management logic (110). The power management logic may monitor assertions of each sentinel node in each logic block. Each time a sentinel node is asserted, a corresponding power number is added to a running total of the current device power estimate.

[0020] The device power estimate may be stored in a one or more registers, latches, or volatile or non-volatile memory. The device power estimate may be calculated over a predetermined time period by adding the number of sentinel node assertions during that time period. In some embodiments, it may be possible to reset the device power estimate as desired.

[0021] By measuring the number of assertions, toggles, or state changes of each sentinel node, the power consumption of each logic block may be estimated by adding a predetermined weighted value to a logic block power total each time the sentinel node for the logic block is asserted and averaged over a pre-defined window of time. Similarly, the power consumption for the entire device may be estimated by monitoring all sentinel nodes, and each time a sentinel node is asserted, adding and averaging the weighted value corresponding to the sentinel node to a device power total. This allows one to estimate device power at runtime.

[0022] Additionally, the assertion counts of each sentinel node may be tracked, for example, by storing the counts in one or more registers, latches, and/or in other volatile or non-volatile memory locations. The assertion counts may be reset as needed to perform any desired power or temperature calculations.

[0023] The power estimate for each logic block and/or for the device as a whole may be used to predict the temperature of the device at runtime using the following equation:

$$T_n=(1-\alpha)*T_{n-1}+(\alpha*k*P_n)$$

[0024] Where, T_n is the temperature of the device at time n, P_n is the average power consumption of the device in the nth time interval, a is the thermal time constant of the device, and k is a scaling constant.

[0025] Using the runtime estimation of device power based on sentinel node assertions, as described above, in conjunction with an initial value for device temperature, this equation may be used to calculate current or future device temperatures, T_n. Furthermore, it may be possible to calculate temperatures for each individual logic block using runtime estimations of logic block power.

[0026] The temperature predictions may be used by the power management logic to throttle device activity on a per-device or per-logic block basis when the calculated device temperature goes above certain predefined threshold values.

[0027] In some embodiments, the sentinel nodes may be used to perform leakage power calculations. In order to ascertain leakage power at runtime, temperature variations in the device or block must be known or estimated. By performing temperature calculations similar to those described above, the estimated temperature values can in turn be used to estimate leakage power at runtime.

[0028] FIG. 2 illustrates a system block diagram according to some embodiments. The system (200) includes at least a processor or CPU (202), memory controller device (206), I/O controller device (218), and one or more memory devices (210). Note that in some embodiments, the memory controller device and/or the I/O controller device may be integrated into the CPU/processor.

[0029] The system may also include a network port or interface (220), and may be capable of being coupled to a wired or wireless network (230). The memory controller device (206) is coupled to the CPU (202) by a bus (204). The memory controller device (206) provides the CPU (202) with access to one or more memory devices (210), to which the memory controller device (206) is coupled by a memory bus (208).

[0030] A graphics processing unit (212) may be coupled to the memory controller device via a bus (214). An I/O controller device (218) may be coupled to the memory controller device (206) by a bus (216). The I/O controller device (218) may be coupled to a network port (220), capable of connecting to a network (230). The I/O controller device (218) may also be coupled to a mass storage device (222) and/or non-volatile memory (224). A battery (203) or other power supply may provide power to the system.

[0031] Together, these components form a system (200) that is capable of supporting the execution of machine readable instructions by CPU (202), and the storage of data, including instructions, within memory devices (210). One or more components in the system may include a plurality of logic blocks, each logic block having one or more sentinel nodes which is monitored by power management logic.

[0032] In one illustrative embodiment, as shown in FIG. 2, the memory controller device includes logic blocks (282). Each logic block includes sentinel nodes (284) which are monitored by power management logic (280). The power management logic (280) may monitor assertions of the sentinel nodes, and may add a corresponding weighted power value to a total device power value each time a sentinel node is asserted, as described above. The power management logic may also track a total power value for each logic block. The device and logic block power information may be used by the power management logic to determine a breakdown of total device power consumption by logic block, and may further be used to calculate a device temperature and/or a logic block temperature. In some embodiments, all or portions of the power management logic may be in another device or chip.

[0033] Using the power consumption and/or temperature information calculated based on sentinel node assertions, the power management logic may be able to take advanced throttling actions, such as throttling the entire memory controller device (**206**), or throttling specific portions of the memory controller device, such as one or more logic blocks, rather than throttling the entire chip.

[0034] In other embodiments, other components of the system may include power management logic and sentinel nodes to monitor and estimate power consumption as described above. These components may include, but are not limited to, the processor (**202**), the I/O controller device (**218**), the graphics processing unit (**212**), or the memory device(s) (**210**). For example, the I/O controller device (**218**) may include a plurality of logic blocks having sentinel nodes coupled to power management logic to monitor the sentinel nodes and calculate device power estimates and/or device temperature.

[0035] FIG. **3** is a flow diagram according to some embodiments of the invention. As shown in block **302**, assertions of a sentinel node in a device are monitored. Sentinel nodes are described in detail above, in conjunction with

FIG. **1**.

[0036] Each time a sentinel node is asserted, a corresponding power number is added to a current power estimate (**304**). For example, for each assertion of a sentinel node, a weighted value corresponding to that particular node may be added to the power estimate. If another sentinel node is asserted, a weighted value corresponding to that sentinel node is added to the power estimate. In this manner, a power estimate may be calculated. The power estimate may be reset periodically, for example, after a predetermined amount of time or after a specified event occurs in the device.

[0037] Additionally, assertion counts for each sentinel node may be tracked and/or stored separately for each logic block. This may allow power estimates to be calculated for portions of the device as well as the device as a whole.

[0038] The power estimate may then be used to calculate an estimated temperature for the device (**306**), as described above in conjunction with FIG. **1**.

[0039] If the power estimate exceeds a predetermined threshold, and/or if the calculated temperature exceeds a predetermined threshold, all or portions of the device may be throttled (**308**). Throttling may include reducing power or reducing power dissipation by the component. Throttling may be done by reducing the operating frequency of a device, reducing power to the device or one or more blocks within the device, disabling one or more logical blocks in the device, or in any other way which would reduce the power or power dissipation of the component.

[0040] Thus, a method, apparatus, and system for runtime power estimation are disclosed. In the above description, numerous specific details are set forth. However, it is understood that embodiments may be practiced without these specific details. In other instances, well-known circuits, structures, and techniques have not been shown in detail in order not to obscure the understanding of this description. Embodiments have been described with reference to specific exemplary embodiments thereof. It will, however, be evident to persons having the benefit of this disclosure that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of the embodiments described herein. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

We claim:

1. A device, comprising:

a first logic block including a first sentinel node, wherein the first sentinel node is to be asserted in response to an architectural event in the first logic block; and

power management logic coupled to the first logic block to add a first value to a power estimate upon an assertion of the first sentinel node.

2. The device of claim 1, wherein the power management logic is further to throttle the device when the power estimate reaches a predetermined value.

3. The device of claim 1, wherein the power management logic is further to throttle the first logic block when the power estimate reaches a predetermined value.

4. The device of claim 1, further comprising a second logic block, including a second sentinel node, coupled to the power management logic, wherein the second sentinel node is to be asserted when an architectural event occurs in the second logic block, and wherein the power management logic is to add a second value to a power estimate based upon an assertion of the second sentinel node.

5. The device of claim 4, wherein the power management logic is further to reset the value of the power estimate after a predetermined time period.

6. The device of claim 4, wherein the power management logic is further to reset the value of the power estimate after a predetermined event occurs.

7. The device of claim 4, wherein the first value is a scaled number representing a capacitance of the first logic block times a squared supply voltage for the first logic block times a clock frequency for the first logic block.

8. The device of claim 4, wherein the second value is a scaled number representing a capacitance of the second logic block times a squared supply voltage for the second logic block times a clock frequency for the second logic block.

9. The device of claim 1, wherein the power management logic is further to calculate a temperature using the power estimate.

10. A system, comprising:

a processor;

a memory controller device coupled to the processor, the memory controller device including power management logic coupled to a plurality of logic blocks, wherein each logic block includes a sentinel node; and

a battery to provide power to the processor and the memory controller device.

11. The system of claim 10, wherein the memory controller device is integrated into the processor.

12. The system of claim 10, wherein the power management logic is to monitor assertions of the sentinel nodes, and is to add a value to a power estimate upon each assertion.

13. The system of claim 12, wherein the value to be added to the power estimate corresponds to a particular sentinel node.

14. The system of claim 10, wherein the power management logic is further to throttle the memory controller device when the power estimate reaches a predetermined threshold value.

15. The system of claim 10, wherein the power management logic is further to throttle a logic block when the power estimate reaches a predetermined threshold value.

16. The system of claim 10, wherein the system further includes an I/O controller device, the I/O controller device including I/O device power management logic coupled to a plurality of I/O device logic blocks, wherein each I/O device logic block includes a sentinel node.

17. A method comprising:

monitoring assertions of a first sentinel node in a first logic block of a device; and

adding a corresponding first power number to a device power estimate when the first sentinel node is asserted.

18. The method of claim 17, further comprising adding the corresponding first power number to a first logic block power estimate when the first sentinel node is asserted.

19. The method of claim 18, further comprising throttling the first logic block when the first logic block power estimate reaches a predetermined threshold value.

20. The method of claim 15, further comprising monitoring assertions of a second sentinel node in a second logic block of a device; and

adding a corresponding second power number to the device power estimate when the second sentinel node is asserted.

21. The method of claim 20, further comprising throttling the device when the device power estimate reaches a predetermined threshold value.

22. The method of claim 17, further comprising resetting the device power estimate after a predetermined time period.

23. The method of claim 18, further comprising resetting the logic block power estimate after a predetermined time period.

24. The method of claim 17, further comprising calculating a temperature of the device based on the device power estimate.

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