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EXAMINER
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte KUN JI and ZHEN SONG

Appeal 2015-007589
Application 13/415,897
Technology Center 2100

Before JEAN R. HOMERE, DANIEL J. GALLIGAN, and
ADAM J. PYONIN, *Administrative Patent Judges*.

PYONIN, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1–18, which are all of the pending claims in the appeal. *See* App. Br. 2. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

STATEMENT OF THE CASE

Introduction

Appellants' invention is directed "to a verification and validation process and system for providing objective assessment of the complete

lifecycle of the redundancy software associated with" programmable logic controllers (PLCs), which "are considered as a special type of computer used in automation systems." Spec. ¶¶ 2–3. Claims 1 and 10 are independent. Claim 1 is reproduced below for reference (App. Br. 11):

> 1. A non-transitory computer readable medium including programming instructions for performing verification and validation of redundancy software included within a finite state machine of a programmable logic control (PLC) redundancy management component, comprising programming instructions for:
>
> processing an initial set of requirements defining PLC redundancy control within the finite state machine to create a feature specification, the processing including a comparison of the initial redundancy requirements and the created feature specification to verify and validate that all redundancy requirements are properly represented in the feature specification for the finite state machine;
>
> processing the feature specification to generate a related architecture specification of software components capable of performing the defined features and a detailed design document of each software component, including a comparison of the feature specification and the architecture specification and detailed design documents to verify and validate that all features are properly represented in the architecture specification and associated detailed design documents, the collection of software components defining the architecture of the finite state machine;
>
> capturing a finite state machine design from the detailed design documents and verifying the finite state machine design;
>
> creating finite state machine source code modules from the detailed design documents, wherein each finite state machine source code module is iteratively tested to perform verification and validation until each module passes verification and validation, providing verification and validation of a complete state space of the finite state machine; and
>
> integrating the finite state machine with the redundancy management component of the PLC system, including

performing verification and validation of the operation of the finite state machine within the PLC system.

References and Rejections

Claims 1–18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cheon et al., *The Software Verification and Validation Process for a PLC-based Engineered Safety Features-Component Control System in Nuclear Power Plants*, The 30th Annual Conference of the IEEE Industrial Electronics Society, November 2–6, 2004, pp 827–831 (hereinafter, "Cheon") and Alur (US 5,483,470; Jan. 9, 1996). Final Act. 4.

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' arguments.[1] We adopt the Examiner's findings and conclusions as our own, and we add the following primarily for emphasis.

A. Iterative Testing

Appellants argue the Examiner erred in finding the cited references teach or suggest "a process step of 'iteratively' testing each 'finite state machine source code module ... until each module passes verification and validation, providing verification and validation of a complete state space of the finite state machine'" as required by claim 1. App. Br. 7–8. In particular, Appellants contend "the 'testing' of the finite state machine in Alur et al is interactive, not 'iterative', as that term is used in independent

[1] We refer to the Final Rejection (mailed November 20, 2013), the Appeal Brief (filed April 17, 2014), the Answer (mailed July 14, 2014), and the Reply Brief (filed December 4, 2014) for the respective details.

claims 1 and 10. That is, the arrangement of Alur et al. essentially performs a manual type of testing, where the 'user' is presented with a diagnostic message and reacts to continue the testing." *Id.* at 8.

We are not persuaded of Examiner error. We agree with the Examiner that Alur teaches iteratively testing a finite state machine, within the meaning of the claim, because Alur discloses "an iterative method of verifying" (Alur 2:27–28), which iterates until "no errors are detected" (Alur 4:20–21). Further, to the extent Appellants' argument relies on Alur's disclosure of user notifications (*see, e.g.*, App. Br. 8), we find Appellants do not persuasively show the claim precludes such user interaction, nor do Appellants persuade us that broadly providing an automatic way to replace a manual activity accomplishing the same result sufficiently distinguishes the claims over the prior art. *See In re Venner*, 262 F.2d 91, 95 (CCPA 1958).

Accordingly, we are not persuaded the Examiner erred in finding the cited references teach or suggest the disputed limitations.

B. Teaching Away

Appellants argue "Alur et al. is considered to <u>teach away</u> from performing verification and validation for the 'complete state space' and, instead, mentions the utilization of a 'reduction' process to eliminate the testing of every state, and instead focus on a few blocks." App. Br. 9. Appellants further contend "[t]he 'state space' is not reduced in the Alur system; the 'reduction' is applied to recognize only that portion of the state space associated with the 'enque-msg' task, and then only test that portion." Reply Br. 2.

We are not persuaded of error. We note Alur's reduction techniques are optional, and do not discourage investigation into the invention claimed. *See* Ans. 7; *see also DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) ("A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not 'criticize, discredit, or otherwise discourage' investigation into the invention claimed.") (citations removed). We find Alur *suggests* testing each module and providing verification and validation of a complete state space within the meaning of the claim because Alur discloses that testing iterates until there are no errors. *See* Ans. 7; Alur 3:65–4:30.

Further, we agree with the Examiner that the claims do not require a specific complexity level of the finite state machine, and "Alur performs validation and verification on all the finite state machine modules in the resulting simpler system," or for "[s]ystems that are not too complicated." Ans. 7. Accordingly, we agree with the Examiner that "the claims do not preclude the reduction techniques disclosed in Alur." Ans. 6.

CONCLUSION

We are not persuaded the Examiner erred in finding the cited references teach or suggest the limitations of independent claim 1, and the limitations of independent claim 10 which are similar in scope. *See* App. Br. 7. We sustain the Examiner's rejection of the independent claims, and dependent claims 2–9 and 11–18, which are not separately argued. *See* App. Br. 10.

DECISION

The Examiner's rejection of claims 1–18 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED