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IBM Corp. (WIP) c/o Walder Intellectual Property Law, P.C. 17304 Preston Road Suite 200 Dallas, TX 75252			HUISMAN, DAVID J	
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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* ALEXANDRE E. EICHENBERGER, BRUCE M. FLEISCHER,  
and MICHAEL K. GSCHWIND

Appeal 2015-006825  
Application 12/250,584<sup>1</sup>  
Technology Center 2100

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Before JEAN R. HOMERE, JOHN A. EVANS, and  
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants seek our review under 35 U.S.C. § 134(a) of the Examiner's Final Rejection of claims 1–3, 5–12, 14, 17–23, and 25, which constitute all of the claims pending in this appeal. Claims App'x. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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<sup>1</sup> Appellants identify the real party in interest as International Business Machines Corp. App. Br. 2.

*Appellants' Invention*

Appellants invented a method and apparatus for dynamic data driven alignment and data formatting in a floating point Single Instruction Multiple Data (SIMD) architecture. Spec. ¶ 2. In particular, a floating point vector register file (330) utilizes a permute unit (710, 720, 730, 740) to perform an all-to-all permutation operation on input operands received from floating point vector registers (760, 770) based on a control vector (780) containing a plurality of vector elements, each having a floating point value including a mantissa and an exponent such that any vector element of any input operand may be selected for storing any vector element of the result register (750). *Id.* ¶¶ 81–86, Figs. 3, 7.

*Illustrative Claim*

Independent claim 1 is illustrative, and reads as follows:

1. An apparatus, comprising:  
a floating point vector register file containing at least two floating point registers;  
a permute unit coupled to the floating point vector register file, the permute unit having at least two operand inputs for receiving input operands containing data to be permuted from the at least two floating point registers, the at least two floating point registers being vector registers each having at least four vector elements, and at least one control vector input for receiving a control vector indicating a permutation pattern as a floating point vector, the control vector comprising a plurality of control vector elements, wherein each of the vector elements of the at least two floating point registers, and each of the

control vector elements of the control vector, stores a floating point value comprising a mantissa and an exponent; and a result vector register coupled to the permute unit, wherein the permute unit generates a result output, that is stored in the result vector register, based on a permutation operation performed by the permute unit on the input operands according to the control vector, wherein the permutation operation provides an all-to-all permutation of the input operands such that any vector element of any of the input operands may be selected for storing in any vector element of the result vector register, wherein each control vector element of the control vector comprises exponent bits and mantissa bits, and a portion of the permutation pattern associated with each control vector element of the control vector is encoded by way of at least one of high-order mantissa bits of the mantissa bits of that control vector element and an exponent value of the exponent bits of that control vector element, or low-order mantissa bits of the mantissa bits of the control vector element and an exponent value of the exponent bits of that control vector element.

*Prior Art Relied Upon*

Roussel et al.	US 6,041,404	Mar. 21, 2000
Moyer	US 7,962,718 B2	June 14, 2011

*Rejections on Appeal<sup>2</sup>*

Claim 25 stands rejected under 35 U.S.C. § 112 (pre-AIA), second paragraph as being indefinite for failing to particularly point out the subject matter which Appellants regard as the invention. Final Rej. 5–6.<sup>3</sup>

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<sup>2</sup> The rejection of claims 1–3, 5–12, 14, and 17–23 under 35 U.S.C. § 112, second paragraph has been withdrawn by the Examiner. Ans. 2 (citing Advisory Action mailed 12/5/2014).

<sup>3</sup> Ans. 2 (citing Final Act. 6 ¶ 20, 1<sup>st</sup> bullet indicating the recitation “the at least one floating point value” in line 7 of claim 25 lacks antecedent basis.)

Claims 1–3, 5–12, 14, 17–23, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Roussel and Moyer. Final Rej. 6–18.

## ANALYSIS

### *Indefiniteness Rejection*

Regarding claim 25, Appellants argue because the phrase “the at least one floating point value” is directed to the at least one floating point value for each of the two operand inputs previously recited in the claim, the cited phrase does not lack antecedent basis. App. Br. 6, Reply Br. 2.<sup>4</sup> This argument is persuasive.

We do not agree with the Examiner that the cited phrase lacks antecedent basis. Ans. 2. As persuasively argued by Appellants, the ordinarily skilled artisan would have readily been apprised of the scope of the cited phrase by reasonably construing “the floating point values” as being values for each of the two input operands previously recited in the claim. Accordingly, we do not sustain the indefiniteness rejection of claim 25.

### *Obviousness Rejection*

Regarding the rejection of claim 1, Appellants argue the proposed combination of Roussel and Moyer does not teach or suggest a permute unit that operates on floating point values in floating point registers based on a control vector having vector elements with floating point values including a mantissa and an exponent stored in the floating point registers. App. Br. 8.

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<sup>4</sup> Rather than reiterate the arguments of Appellants and the Examiner, we refer to the Appeal Brief (filed January 9, 2015), the Reply Brief (filed July 10, 2015) and the Answer (mailed May 11, 2015) for their respective details.

In particular, Appellants argue Roussel does not teach a permute unit having a control vector input for receiving a control vector indicating a permutation pattern as a floating point vector. Instead, Roussel teaches multiplexers for shuffling with an “8 bit immediate value.” *Id.* at 9 (citing Roussel 5:53–68). Because an “immediate value” is an integer value encoded in an instruction containing bits to indicate which operation to perform in which input registers, Roussel’s multiplexer does not teach any control input. *Id.* at 9–13. Further, Appellants argue that Moyer discloses a destination register storing in its original state indices in hexadecimal format for selecting bytes from registers rA and rB (0-7 in rA, and 8-F in rB), thereby overwriting hexadecimal indices in original destination registers with corresponding values from rA and rB. *Id.* at 13–14. Consequently, Appellants submit that the proposed combination of Roussel with Moyer would at best result in integer control values being implemented as hexadecimal index values from registers rA and rB. According to Appellants, the combination would still lack the disputed control vector as set forth in the claim. *Id.* at 14. These arguments are persuasive.

At the outset, we note that the claim requires a control vector containing a plurality of vector elements, each storing a floating point value including a mantissa and an exponent in at least two floating point registers. While the Examiner correctly finds that Roussel discloses floating point registers, and Moyer discloses a permutation using more flexible control vectors, we do not agree with the Examiner that the proposed combination teaches the specific control vector required by the claim. *Ans.* 7–8. At best, the combination of Roussel and Moyer would result in a control vector containing a single control vector element having values that may be stored

in Roussel's floating point registers. However, the proposed combination would still fall short of teaching or suggesting two or more vector elements in each control vector, wherein each of the vector elements includes floating point values that are stored in the floating point registers. Because Appellants have shown at least one reversible error in the Examiner's obviousness rejection, we need not reach Appellants' remaining arguments. Consequently, we reverse the Examiner's rejection of claim 1, as well as claims 2, 3, 5–12, 14, 17–23, and 25, which recite the disputed limitations discussed above.

#### DECISION

We reverse the Examiner's rejections of claims 1–3, 5–12, 14, 17–23, and 25 as set forth above.

REVERSED