



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
13/559,128 07/26/2012 James Saloio JR. PA0022918U-U100.12-431KL 1089

88326 7590 11/23/2016
Kinney & Lange, P.A.
The Kinney & Lange Building
312 South Third Street
Minneapolis, MN 55415

EXAMINER

POTHEN, FEBA

ART UNIT PAPER NUMBER

2868

NOTIFICATION DATE DELIVERY MODE

11/23/2016

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPatDocket@kinney.com
smkomarec@kinney.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JAMES SALOIO, JR. and JAMES A. GOSSE

Appeal 2015-006537
Application 13/559,128
Technology Center 2800

Before LINDA M. GAUDETTE, WESLEY B. DERRICK, and BRIAN D. RANGE, *Administrative Patent Judges*.

RANGE, *Administrative Patent Judge*.

DECISION ON APPEAL

SUMMARY

Appellants¹ appeal under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 1–18. We have jurisdiction. 35 U.S.C. § 6(b).

We REVERSE.

¹ According to the Appellants, the real party in interest is Hamilton Sundstrand Corporation. Appeal Br. 2.

STATEMENT OF THE CASE

The present application is a continuation-in-part of Application No. 13/401,053. Appeal Br. 2.² Appellants also appealed from the rejection of the claims in that application. *See* Appeal No. 2015-006468.

Appellants describe the invention as relating to testing over-current fault detection in the field. Spec. ¶ 2. In particular, the invention includes a monitor circuit, microcontroller, and resistor configured to test over current. *Id.* at ¶ 15. Appellants' Specification explains that, in the past, over-current fault detection required applying an external fault to the system such that over-current fault handling could not be tested in the field. *Id.* at ¶ 5. Claims 1 and 11, reproduced below with emphases added to certain key recitations, are the only independent claims on appeal and are illustrative of the claimed subject matter:

1. A system for testing over-current fault detection comprising:
 - a first switch to connect a voltage to a load and a capacitor;
 - a first monitor circuit that monitors a current from the first switch to the load;
 - a second monitor circuit that monitors a voltage across the capacitor; and
 - a microcontroller configured to control a state of the first switch to connect voltage to the load to test the first monitor circuit based upon in-rush current generated during charging of the capacitor**, wherein the microcontroller detects an over-current fault condition based upon input from the first monitor circuit, and wherein the microcontroller detects a short-

² In this decision, we refer to the Final Office Action mailed September 12, 2014 ("Final Act."), the Appeal Brief filed February 18, 2015 ("Appeal Br."), the Examiner's Answer mailed April 27, 2015 ("Ans."), and the Reply Brief filed June 26, 2015 ("Reply Br.").

circuit fault condition based upon input from the second monitor circuit during the test of the first monitor circuit.

11. A method for testing over-current fault detection comprising:

- a. enabling a first switch for a predefined time in order to provide voltage to charge a capacitor;
- b. **monitoring, during a test of the over-current fault detection**, an in-rush current from the first switch to the capacitor using a first monitor circuit;
- c. monitoring a voltage across the capacitor using a second monitor circuit;
- d. indicating an over-current fault condition if the in-rush current is larger than a specified value for the predefined time; and
- e. indicating a short-circuit fault condition if the voltage across the capacitor is less than a reference voltage.

Appeal Br. 10–12 (Claims Appendix).

REFERENCES

The Examiner relies upon the prior art below in rejecting the claims on appeal:

Suzuki et al., (hereinafter “Suzuki”)	US 7,843,706 B2	Nov. 30, 2010
Smart et al., (hereinafter “Smart”)	US 8,699,356 B2	Apr. 15, 2014
Fukushi et al., (hereinafter “Fukushi”)	US 2010/0181984 A1	July 22, 2010
Davis et al., (hereinafter “Davis”)	US 2011/0194217 A1	Aug. 11, 2011
Linder	US 2012/0116482 A1	May 10, 2012

REJECTIONS

The Examiner maintains the following rejections on appeal:

Rejection 1. Claims 1, 7–11, 16 and 17 under 35 U.S.C. § 103 as unpatentable over Fukushi in view of Suzuki. Final Act. 3.

Rejection 2. Claims 2–5 and 13–15 under 35 U.S.C. § 103 as unpatentable over Fukushi in view of Suzuki in further view of Smart. *Id.* at 6.

Rejection 3. Claim 6 under 35 U.S.C. § 103 as unpatentable over Fukushi in view of Suzuki in further view of Linder. *Id.* at 9.

Rejection 4. Claim 12 under 35 U.S.C. § 103 as unpatentable over Fukushi in view of Suzuki in further view of Davis. *Id.*

Rejection 5. Claim 18 under 35 U.S.C. § 103 as unpatentable over Fukushi in view of Suzuki in further view of Linder. *Id.* at 10.

ANALYSIS

The Examiner rejects claims 1 and 11—the independent claims—as obvious over Fukushi in view of Suzuki. Final Act. 3. Appellants argue that neither Fukushi nor Suzuki teach “a microcontroller configured to control a state of the first switch to connect voltage to the load to test the first monitor circuit based upon in-rush current generated during charging of the capacitor” as recited in claim 1 and that neither of these references teach similar elements of claim 11. Appeal Br. 6–7. A preponderance of the evidence supports the Appellants’ position.

The Examiner construes testing as “an evaluation or a means by which the presence of anything is determined” and then finds that Fukushi teaches detecting an overcurrent in a system using a circuit and thus teaches

testing or determining the presence of an overcurrent. Dec. 15, 2014, Advisory Action. Both claims 1 and 11, however, require more than testing for the presence of an overcurrent; claim 1 requires a microcontroller configured to control a switch configured “to test the first monitor circuit based upon in-rush current generated during charging of the capacitor,” and claim 11 requires “monitoring, during a test of the over-current fault detection.” Appeal Br. 10–12 (Claims Appendix). In other words, each claim is directed, at least in part, to an apparatus (claim 1) or a method (claim 11) relating to testing of the over-current detection apparatus itself.

The Examiner also finds that “[t]he fact that the amplifier 72 of the overcurrent circuit 70 outputs a value and drives the circuitry for activating/[]deactivating the switch q1 is an evaluation [i.e., a test] of the circuit.” Ans. 2. Appellants, however, persuasively explain that Fukushi’s amplifier 72 providing an output is not the same as testing the overcurrent circuit 70 as recited by claim 1 because Fukushi does not disclose evaluating whether or not the overcurrent detection is working properly. Reply Br. 2. In other words, even if Fukushi’s amplifier circuit attempts to detect overcurrent and provides a corresponding output, Fukushi does not teach any evaluation of whether or not the detection and output is correct. Similarly, with respect to claim 11, the Examiner identifies testing for over-current in Fukushi but not “a test of the over-current fault detection.” Appeal Br. 8–9.

The Examiner also finds that Suzuki discloses “test[ing] the first monitor circuit” (Ans. 4), finds that Suzuki controls a switch based upon detection of an in-rush current (*i.e.*, a form of overcurrent) (*id.*), and finds that Suzuki teaches “a short circuit fault condition based upon input from a second monitor circuit, which is shown by voltage sensor [*sic*, sensor] 9 in

Fig. 1 of Suzuki” (*id.* at 5). Appellants, however, persuasively explain that Suzuki limits in-rush current but does not teach a controller or control circuit that evaluates/tests the overcurrent detection circuit. Ans. 6; Reply Br. 2; *see also* Suzuki Title. Appellants further explain, for example, that sensor 9 of Suzuki’s Figure 1 monitors voltages across capacitor 3 and resistor 2 so that ECU 6 may limit in-rush current (Appeal Br. 7 (citing Suzuki 16:30–45)). A preponderance of the evidence supports Appellants’ position. *See, e.g.,* Suzuki 15:40–58 (explaining that sensor 9 is a part of the inrush current limiting circuit).

Based on the present record, the Examiner has not directed us to sufficient factual underpinnings to support a determination that it would have been obvious to implement, in conjunction with claim 1’s other recitations, “a microcontroller configured to control a state of the first of the first switch to connect voltage to the load to test the first monitor circuit based upon in-rush current generated during charging of the capacitor” or that it would be obvious to implement, in conjunction with claim 11’s other recitations, “monitoring, during a test of the over-current fault detection, an in-rush current.” *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Accordingly, we do not sustain the Examiner’s rejection of claims 1 and 11. We also do not sustain the Examiner’s rejection of claims 7–10, 16, and 17 because those claims depend from claims 1 and 11.

The Examiner applies additional references to dependent claims 2–6, 12–15, and 18, but the Examiner does not determine that these references teach or render obvious the recitations of claims 1 and 11 discussed above. Final Act. 6–10. For example, although the Examiner applies Davis to claim 12 and finds that Davis teaches “indicating a failed test if an over-current condition was not indicated” (Final Act. 9–10 (citing Davis ¶ 49)), the Examiner does not rely on Davis as teaching or rendering obvious the elements of claims 1 and 11.³ We therefore do not sustain the Examiner’s rejection of claims 2–6, 12–15, and 18.

DECISION

For the above reasons, we reverse the Examiner’s rejections of claims 1–18.

REVERSED

³ In the event of further prosecution, the Examiner may wish to consider whether or not a person of skill in the art at the relevant time would have applied Davis in combination with other references and whether or not such a combination would have rendered the recitations of claim 1 and/or claim 11 obvious.