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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ARMAGAN AKAR and RALPH SANCHEZ

Appeal 2015-006506
Application 13/150,964
Technology Center 2800

Before KAREN M. HASTINGS, CHRISTOPHER C. KENNEDY, and BRIAN D. RANGE, *Administrative Patent Judges*.

RANGE, *Administrative Patent Judge*.

DECISION ON APPEAL

SUMMARY

Appellants[1] appeal under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 1–22. We have jurisdiction. 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

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[1] According to the Appellants, the real party in interest is Teseda Corporation. Appeal Br. 3.

STATEMENT OF THE CASE

Appellants describe the invention as relating to identifying defect locations or regions in integrated circuits ("ICs") based on electrical logic testing of the integrated circuits. Appeal Br. 3. Appellants explain that the invention would allow a back end IC manufacturer to identify defect locations without access to the detailed circuit design of the IC design company. *Id.* Claim 1, reproduced below with emphasis added to certain key recitations, is illustrative of the claimed subject matter:

> 1. A method for identifying a candidate physical defect region including a physical defect in a failing semiconductor device, the method comprising:
>
> receiving plural electrical test mismatch results reported for one or more scan chains of the failing semiconductor device;
>
> at a failure analysis computing device, generating a physical representation of a portion of the failing semiconductor device, the physical representation including a mapping of physical layout **to provide location information for physical instantiations of circuit cells represented as polygon areas and physical interconnections linking the polygon areas, each circuit cell represented as a polygon area including logic circuitry that performs logical operations**;
>
> identifying for each electrical test mismatch result a suspect logical region and interconnections that are electrically connected with the scan chain and correspond to the electrical test mismatch result;
>
> identifying the candidate physical defect region as one or more of a polygon area and an interconnection, the candidate physical defect region corresponding to an overlap of one or more polygon areas and interconnections in the suspect logical regions of the plural electrical test mismatch results; and
>
> displaying the candidate physical defect region as one or more of a polygon area and an interconnection in the physical representation of a portion of the failing semiconductor device.

Appeal Br.[2] 10 (Claims Appendix).

REJECTION

On appeal, the Examiner maintains the rejection of claims 1–22 under 35 U.S.C. § 103 as unpatentable over Rajski et al. (US 2006/0053357 A1, March 9, 2006) (hereinafter "Rajski") in view of Reilly et al. (U.S. Patent No. 8,141,026, March 9, 2006) (hereinafter "Reilly").

ANALYSIS

Claims 1–14, 17–20, and 22. The Examiner rejects independent claims 1 and 17 as obvious over Rajski in view of Reilly. The Examiner finds that Rajuski discloses a method for identifying defect regions of a semiconductor device but does not explicitly disclose, for example, providing "location information for physical instantiations of circuit cells represented as polygon areas" as recited by claims 1 and 17. Final Act. 3. The Examiner finds, however, that Reilly supplies this missing element via its Figure 5 and related text. *Id.* Appellants respond by arguing that that Reilly does not disclose "location information for physical instantiations of circuit cells represented as polygon areas." Appeal Br. 8.

We begin our analysis with claim construction of the recitation "physical instantiations of circuit cells represented as polygon areas" as it appears in claim 1. The Specification explains that this refers to polygons forming the boundaries of physical space:

[2] In this decision, we refer to the Final Office Action mailed December 19, 2013 ("Final Act."), the Appeal Brief filed November 19, 2014 ("Appeal Br."), the Examiner's Answer mailed April 20, 2015 ("Ans."), and the Reply Brief filed June 19, 2015 ("Reply Br.").

> In a placement and routing phase 114, the various logical cells of design implementation 110 may be rendered as polygons. Such polygons represent "footprints" for the physical instantiations of the logical cells in the physical layout of the device. In other words, polygons form the boundaries of the physical space that a device structure will occupy when the physical layout is rendered in silicon.

Spec. ¶ 32. Thus, the "polygon areas" portion of the recitation "physical instantiations of circuit cells represented as polygon areas" must represent particular boundaries and dimensions of the real world physical silicon. This is not the same as, for example, polygon areas that merely identify or group real world components as a diagram without being tied to real boundaries and dimensions of physical real world space. *See also* Reply Br. 3.

Claim 17 recites "generat[ing] a physical representation of a portion of the failing semiconductor device, the physical representation comprising location information for polygons that represent circuit cells and location information for interconnections between the circuit cells." Given the context provided by the Specification discussed above and given the recitations of claim 17 (reciting, e.g., "location information for polygons"), we likewise construe the polygons of claim 17 as representing particular boundaries and dimensions of real world silicon (and including circuit cells and location information for interconnections between the circuit cells).

Based on this claim construction, the Examiner's finding that Figure 5 of Reilly discloses "physical instantiations of circuit cells represented as polygon areas" (Final Act. 4; Ans. 4) is erroneous. Appeal Br. 8. Rather, a preponderance of the evidence suggests that Figure 5 of Reilly provides a diagram or illustration of different components rather than polygons

representing actual real-world boundaries and dimensions of the physical rendered semiconductor. Ans. 8. Figure 5 of Reilly is reproduced below:

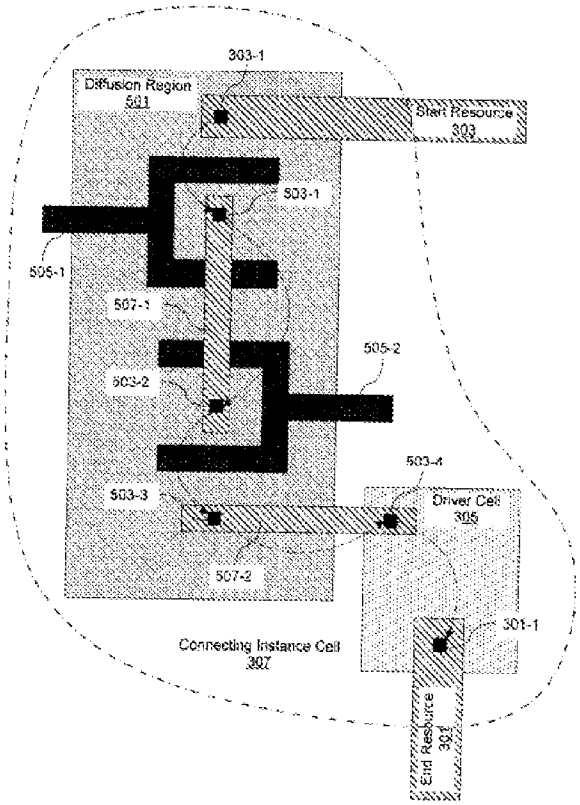

Fig. 5

Reilly Figure 5 "is a block diagram illustrating an exemplary physical signal path." Reilly 2:3–6.

The physical signal path of Figure 5 corresponds to the logical circuit of Reilly's Figure 3. Each polygon in Figure 5 represents a physical component. For example, the largest gray rectangle represents diffusion region 501. Reilly 5:32–57. The topmost solid black polygon represents polysilicon region 505-1. *Id.* The vertically orientated rectangle shaded with diagonal lines represents metal line 507-1. *Id.* The combination of contacts 303-1 and 503-1 and separated by polysilicon region 505-1 satisfy a model for a transitor. *Id.* Thus, each polygon appears to represent a discrete

physical component, and the text of Reilly does not teach or suggest that the polygons corresponds to physical boundaries or dimensions of the real world silicon semiconductor (as opposed to being a diagrammatic representation of real world components). *See also* Appeal Br. 6–8; Reply Br. 3. At most, Reilly Figure 5 may indicate the relative locations of each component (i.e., whether they are connected) (Ans. 6), but this is not the same as forming polygons that correspond to physical boundaries or dimensions of the silicon semiconductor.

The Examiner references Figure 4 as selecting features "from the layout design" (Ans. 5) (emphasis removed), but this only refers to Reilly's algorithm selecting shapes (for example, metal lines) from the physical layout. Reilly 5:10–26. The shapes are then analyzed to see if they match an end resource in order to identify components. *Id*. Thus, as a whole, Reilly appears more focused on analyzing failures based on identifying and assessing functional components rather than assessing polygon areas that correspond to physical boundaries on the semiconductor.

Because a preponderance of the evidence does not support the Examiner's position that the cited references teach or suggest the recitations of claims 1 and 17 concerning polygon areas, we do not sustain the rejection of these claims. We also do not sustain the rejection of claims 2–14, 18–20, and 22 because those claims each depend from claim 1 or 17.

<u>Claims 15, 16, and 21.</u> As explained above, Appellants' argument is based upon the cited references not teaching or suggesting "location information for physical instantiations of circuit cells represented as polygon areas." Appeal Br. 8. Independent claims 1 and 17 recite the polygon areas, but independent claims 15 and 21 and dependent claim 16 do not.

Appellants make no arguments that apply to the recitations of claims 15, 16, or 21. Our review of the appealed rejections is for error based upon the issues identified by Appellants and in light of the arguments and evidence produced thereon. *Cf. Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) (cited with approval in *In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011) ("it has long been the Board's practice to require an applicant to identify the alleged error in the examiner's rejections")). Because Appellants fail to identify reversible error with respect to claims 15, 16, and 21, we sustain the Examiner's rejection of these claims for the reasons expressed by the Examiner in the Final Office Action and the Answer.

DECISION

For the above reasons, we affirm the Examiner's rejection of claims 15, 16, and 21. We reverse the Examiner's rejection of claims 1–14, 17–20, and 22.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART