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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte FREDERICK PERNER

Appeal 2015-006322
Application 13/384,004
Technology Center 2800

Before MAHSHID D. SAADAT, JOHNNY A. KUMAR, and
JON M. JURGOVAN, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant¹ seeks review under 35 U.S.C. § 134(a) from the Final Rejection of claims 1, 3–9, 11–16, and 18–20. Claims 2, 10, and 17 were indicated as containing allowable subject matter. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.²

¹ Appellant identifies Hewlett-Packard Development Company, LP as the real party in interest. (App. Br. 2.)

² Our Decision refers to the Specification filed Jan. 13, 2012 (“Spec.”), the Final Office Action mailed Aug. 11, 2014 (“Final Act.”), the Appeal Brief filed Dec. 11, 2014 (“App. Br.”), the Examiner’s Answer mailed Apr. 16, 2015 (“Ans.”), and the Reply Brief filed June 8, 2015 (“Reply Br.”).

CLAIMED SUBJECT MATTER

The claims are directed to methods and systems for connecting read/write circuitry to a memory structure in a manner that allows for higher density memory arrays. (Spec. ¶ 21.)

Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. An interconnect architecture for connecting read/write circuitry to a memory structure, the interconnect architecture comprising:

a switching layer comprising a number of access switches arranged in at least one set of two offset switch blocks, said access switches being connected to a first set of parallel wire tracks and a second set of parallel wire tracks intersecting said first set of parallel wire tracks; and

a routing layer connecting said access switches to a number of access vias of said memory structure;

in which four wire tracks are used to select a programmable device of said memory structure.

REJECTIONS

Claims 1, 3, 5, 6, 9, 11, 15, 16, and 19 stand rejected under 35 U.S.C. § 102(b) based on Stipe (US 2008/0037349 A1; publ. Feb. 14, 2008). (Final Act. 2–6.)

Claims 4, 12, and 18 stand rejected under 35 U.S.C. § 103(a) based on Stipe and Teig et al. (US 2004/0098696 A1; publ. May 20, 2004). (Final Act. 6–8.)

Claims 7, 13, and 20 stand rejected under 35 U.S.C. § 103(a) based on Stipe and Mouttet (US 2009/0163826 A1; publ. June 25, 2009). (Final Act. 8–9.)

Claims 8 and 14 stand rejected under 35 U.S.C. § 103(a) based on Stipe and Kim et al. (US 2007/0153616 A1; publ. July 5, 2007). (Final Act. 9–10.)

ANALYSIS

35 U.S.C. § 102(b) Rejection over Stipe

Independent Claims 1 and 9

Appellant contends Stipe does not disclose “four wire tracks are used to select a programmable device of said memory structure,” because “a,” the singular article, means that four tracks must be used to select any singular programmable element, and Stipe uses only two lines, a row line and a column line, to select a single memory element. (App. Br. 9–13; Reply Br. 4–6.) Appellant argues claims 1 and 9 require a four dimensional addressing scheme, where “a total of four coordinates indicating four wire tracks are used to select a particular crosspoint in the crossbar array.” (*Id.* at 13 (citing Spec. ¶ 45).)

Appellant’s contention that Stipe does not disclose using four wire tracks to select a crosspoint in the array is not commensurate with the scope of the claims, which do not require selecting a singular “crosspoint.” *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (stating that limitations not appearing in the claims cannot be relied upon for patentability). Under the broadest reasonable interpretation consistent with Appellant’s disclosure, we agree with the Examiner’s finding that “a programmable device” does not preclude reading the claim element on a device comprising a block of memory elements, such as Stipe’s memory trees 302a and 302b.³ (Ans. 2–3

³ The Examiner mistakenly labels Stipe’s memory device sections (i.e., trees) as 320a and 320b (Ans. 3), which are transistor write lines in Figures 3

(citing Stipe Figs. 3 and 4); see *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004): “[T]he PTO is obligated to give claims their broadest reasonable interpretation during examination.”) Further, we agree with the Examiner’s finding that the claims do not require four tracks are needed to select a single element, i.e., there is no requirement that the four tracks be used simultaneously. (Ans. 3.) Thus, we agree that Stipe discloses at least four wire tracks, i.e., the combination of four lines 306 and sixteen lines 307, are used when selecting among the various memory elements 301 within the programmable device tree 302a or 302b (*id.*), and we sustain the rejection of independent claims 1 and 9 under 35 U.S.C. § 102(b) as anticipated by Stipe.

Independent Claim 15

The Examiner finds Stipe discloses two offset switch blocks (Ans. 4 (citing Stipe Fig. 5, column switch block 506 and row switch block 503)), with access switches being connected, through memory cells 301, to a first set of parallel wire tracks 306 and a second set of parallel wire tracks 307 that intersect the first set (*id.* (citing Stipe Figs. 3 and 4)). Appellant contends Stipe’s column switch is only connected to a column line, and a row switch is only connected to a row line, thus Stipe fails to disclose the claimed access switch connected to a first set of parallel wire tracks *and* a second set of parallel wire tracks. (App. Br. 14–16.) Appellant argues connecting the access switches to the sets of parallel wire tracks through the

and 4, not device sections. Nonetheless, we find this to be a harmless error, as the Examiner clearly describes wire tracks 306 being used to select memory elements in the device “sections” (*id.*), where tracks 306 are the branches within trees 302a and 302b.

memory cells would not be a connection that is part of the switching layer, and is not what is intended by the language of claim 15. (Reply Br. 9.)

We are unpersuaded of error in the rejection, as claim 15 only requires the switching layer to comprise the access switches, and does not require the first and second set of parallel wire tracks to be part of the switching layer. Thus, under the broadest reasonable interpretation of the claim consistent with Appellant's disclosure, we agree with the Examiner's finding that the disclosed offset switch blocks (i.e., 503 and 506) comprise access switches that are in electrical connection with a first set (306) and second set (307) of parallel wires through the memory cells. (Ans. 3–4 (citing Stipe Figs. 3 and 4); *see Am. Acad. of Sci. Tech. Ctr., supra.*)

Dependent Claim 19

Appellant contends Stipe does not disclose a “routing layer is configured to route signals from said access switches along two perpendicular lines to connect to access vias of said aligned crossbar array,” because Stipe's connection between switches (i.e., transistors 312) and vias (i.e., 305) is direct and does not include the claimed routing layer. (App. Br. 17; Reply Br. 10–11). We are not persuaded of Examiner error in the rejection. Claim 19 does not require any particular structure for the “two perpendicular lines,” other than a connection between access switches and access vias. Thus, we agree with the Examiner's finding that Stipe's layers 318 and 317, which comprise at least two perpendicular contact portions down to the transistor regions formed in the substrate, are routing layers that route signals between the transistor switches 312 and the array vias 305. (Ans. 4–5 (citing Stipe Figs. 3 and 4).)

*35 U.S.C. § 103(a) Rejection over Stipe and Teig
Dependent Claim 18*

Appellant contends the combination of Stipe and Teig does not teach a “routing layer [that] is configured to route signals from said access switches into a diagonal pattern to access vias of said disjointed crossbar array.” (App. Br. 18.) Appellant argues Teig’s diagonal node edge between groups is not a signal path, and thus cannot be the claimed routing layer. (*Id.*) The Examiner finds, and we agree, that Teig teaches the use of diagonal wiring tracks to route signals between sub-regions of a circuit (Ans. 6–7 (citing Teig ¶¶ 6 and 37)), which can include a memory device (*see also* Teig ¶ 3), in order to improve the efficiency of the interconnect wiring layout. The Examiner further finds that Stipe teaches the claimed “disjointed crossbar array,” as the array plate lines and their vias are formed in an offset, or disjointed, pattern (Ans. 6–7 (citing Stipe ¶ 89 and Fig. 4.)), and Appellant did not challenge this finding. Thus, we agree with the Examiner’s finding that the combination of Stipe and Teig teaches the claimed routing of signals from access switches into a diagonal pattern to access vias of the disjointed cross bar array (Ans. 6–7), and we sustain the Examiner’s rejection of claim 18 under 35 U.S.C. § 103(a).

Remaining Claims

No separate arguments are presented for remaining dependent claims 3–8, 11–14, 16, and 20. Thus, for reasons stated with respect to independent claims 1, 9, and 15, we sustain the Examiner’s rejection of the dependent claims. *See* 37 C.F.R. § 41.37(c)(1)(iv); *In re King*, 801 F.2d 1324, 1325 (Fed. Cir. 1986); *In re Sernaker*, 702 F.2d 989, 991 (Fed. Cir. 1983).

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DECISION

We affirm the Examiner's decision to reject claims 1, 3–9, 11–16, and 18–20 under 35 U.S.C. § 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED