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Medtronic, Inc. (CRDM) 710 MEDTRONIC PARKWAY NE MS: LC340 Legal Patents MINNEAPOLIS, MN 55432-9924			SKIBINSKI, THOMAS S	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte KEVIN K. WALSH and
MELVIN P. ROBERTS¹

Appeal 2015-006112
Application 13/802,877
Technology Center 2800

Before BRADLEY R. GARRIS, ADRIENE LEPIANE HANLON, and
JULIA HEANEY, *Administrative Patent Judges*.

GARRIS, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134, Appellants appeal from the Examiner's rejections of independent claims 1, 12, 16, and 25 as well as dependent claims 2–7, 11, 13, 14, and 17–21 under 35 U.S.C. § 102(b) as anticipated by Inoue et al., (US 6,216,256 B1 issued Apr. 10, 2001; hereinafter “Inoue”) and of dependent claims 8–10 and 15 under 35 U.S.C. § 103(a) as unpatentable over Inoue. We have jurisdiction under 35 U.S.C. § 6.

¹ MEDTRONIC, INC. is identified as the real party in interest. App. Br. 3.

We REVERSE.

Appellants claim an integrated circuit, as well as a device and method involving such a circuit, comprising a plurality of clocked components 58, each of which includes a data signal transmission path 75 having a clocked component delay element 76, wherein each of the clocked components comprises a flip-flop and the data signal transmission path is defined between an input terminal and an output terminal of each flip-flop (independent claim 1, Fig. 4; *see also* remaining independent claims 12, 16, and 25).

A copy of representative claim 1, taken from the Claims Appendix of the Appeal Brief, appears below.

1. An integrated circuit, comprising:
 - a clock source for generating a clock signal;
 - a clock tree having a plurality of clock lines distributed within the integrated circuit for transmission of the clock signal;
 - a plurality of clocked components, wherein each of the clocked components includes a data signal transmission path having a clocked component delay element and being connected to one of the plurality of clock lines;
 - a first data signal line coupled between a data output of a transmitting clocked component of the plurality of clocked components and a data input of a receiving clocked component of the plurality of clocked components;
 - and
 - a clock tree delay element coupled to a clock line of the receiving clocked component to generate a modified clock signal, wherein the transmitting clocked component is configured to output the data subsequent to reception of the modified clock signal by the receiving clocked component, and

wherein each of the plurality of clocked components comprises a flip-flop, and the data signal transmission path of each of the plurality of clocked components is defined between an input terminal and an output terminal of each flip-flop.

Appellants contest the § 102 rejection of the independent claims by arguing that “Inoue’s delay element 202 resides externally in relation to the flip-flop F21” (App. Br. 9) whereas the independent claims require a clocked component delay element between the input terminal and the output terminal of the flip-flop (*id.*).

In response, the Examiner provides an annotated copy of flip-flop 58c depicted in Appellants’ Figure 4 wherein electrical components to the left of delay element 76 are characterized by the Examiner as “Flip-Flop Function Elements” (Ans. 14). According to the Examiner, “[b]oth Figure 7 of Inoue and 58c of Figure 4 of Appellant[s]’ application disclose a circuit performing the function of a flip-flop with a delay element directly connected to the output of the flip-flop function element” (*id.*). The Examiner determines that, “[g]iven broadest reasonable interpretation, the delay element 202 of Figure 7 of Inoue could be considered part of the transmission path between the input and output of the flip-flop F21 in the same way the delay element 76 of the instant application is considered to be part of the transmission path 75 of the flip-flop function element of 58c of Figure 4 of Appellant[s]’ application” (*id.*).

The Examiner’s position lacks persuasive merit for a number of reasons. First, the Examiner offers no support for characterizing as “flip-

flip function elements” the electrical components to the left of delay element 76 in flip-flop 58c of Appellants’ Figure 4. Second, the Examiner likewise offers no support for regarding these “flip-flop function elements” as corresponding to Appellants’ claimed flip-flop or Inoue’s flip-flop F21. Finally, the Examiner does not explain why the independent claim requirement of a clocked component delay element located between the flip-flop’s input and output terminals is satisfied by delay elements which are external to the input and output terminals of the “flip-flop function elements” shown in Appellants’ Figure 4 and the flip-flop F21 shown in Inoue’s Figure 7.

For the above-stated reasons, the Examiner fails to establish a prima facie case of anticipation for the independent claims on appeal. We do not sustain, therefore, the Examiner’s § 102 and § 103 rejections.

The decision of the examiner is reversed.

REVERSED