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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte HERIBERT LINDLAR and STEFAN SATTLER¹

Appeal 2015-006062
Application 12/097,463
Technology Center 2800

Before BRADLEY R. GARRIS, GEORGE C. BEST, and WESLEY B. DERRICK, *Administrative Patent Judges*.

GARRIS, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134, Appellants appeal from the Examiner's rejections under 35 U.S.C. § 103(a) of claims 1–14, 17, and 18 over AAPA (Appellants' Admitted Prior Art (Fig. 4, Spec. 2–3)) in combination with Jackson (US 2004/0051384 A1, published Mar. 18, 2004) (Final Action 3–8) and claims 19–22 as unpatentable over this combination in further view of

¹ Nokia Corporation of Espoo, Finland is identified as the real party in interest. App. Br. 2.

Choi (US 2006/0256589 A1, published Nov. 16, 2006) (*id.* at 8–10). We have jurisdiction under 35 U.S.C. § 6.

We AFFIRM.

Appellants claim control circuitry configured to, in response to receiving a first value, control a switch to connect a bus line to a charge storage device and, in response to receiving a second value, control the switch to disconnect the bus line from the charge storage device (independent claim 1; *see also* independent claims 8 and 11). Appellants also claim a corresponding method for controlling a switch (independent claim 12) and a non-transitory computer-readable medium storing program code configured to effect such switch control (independent claim 14).

A copy of representative claims 1, 12, and 18, taken from the Claims Appendix of the Appeal Brief, appears below.

1. Control circuitry configured to:
 - receive data represented by voltage levels over a bus line configured to transfer data and power between peripheral device circuitry and terminal device circuitry;
 - in response to receiving a first value of data represented by a first voltage level from the terminal device circuitry over the bus line, control a switch to connect the bus line to a charge storage device of the peripheral device circuitry such that power is supplied to the charge storage device over the bus line, wherein the charge storage device is configured to receive power from the terminal device circuitry over the bus line and to supply power to the control circuitry; and
 - in response to receiving a second value of data represented by a second voltage level from the terminal device circuitry over the bus line, control the switch to disconnect the

bus line from the charge storage device and prevent the charge storage device from discharging power over the bus line.

12. A method comprising
in response to receiving a first value of data represented by a first voltage level from terminal device circuitry over a bus line configured to transfer data and power between peripheral device circuitry and the terminal device circuitry, controlling, by control circuitry, a switch to connect the bus line to a charge storage device of the peripheral device circuitry such that power is supplied to the charge storage device over the bus line, wherein the charge storage device is configured to receive power from the terminal device circuitry over the bus line and to supply power to the control circuitry; and
in response to receiving a second value of data represented by a second voltage level from the terminal device circuitry over the bus line, controlling, by the control circuitry, the switch to disconnect the bus line from the charge storage device and prevent the charge storage device from discharging power over the bus line.

18. The method of claim 12, wherein the bus line is configured to transfer digital data and the power between the peripheral device circuitry and the terminal device circuitry, wherein the first voltage level is a logic high voltage level for signaling digital data via the bus line, and wherein the second voltage level is a logic low voltage level for signaling digital data via the bus line.

App. Br. 24, 27, 28 (Claims Appendix).

Appellants present arguments regarding independent claim 1 (App. Br. 8–13) and reiterate these arguments for remaining independent claims 8, 11, 12, and 14 (*id.* at 13–16). Appellants also present separate arguments concerning dependent claims 18–22 (*id.* at 16–22). The other dependent

claims have not been separately argued and therefore will stand or fall with their argued parent claims.

We sustain the above rejections based on the findings of fact, conclusions of law, and rebuttals to arguments well expressed by the Examiner in the Final Action and Answer. The following comments are added for emphasis and completeness.

In rejecting claim 1, the Examiner finds that the AAPA circuit includes a diode, instead of a controlled switch as claimed, for connecting and disconnecting a bus line and a charge storage device (Final Action 3–4). Regarding this deficiency, the Examiner finds that Jackson discloses replacing a diode with a switch to achieve the same or similar functionality (*id.* at 4). In light of these findings, the Examiner concludes that it would have been obvious “to have modified the control circuitry of AAPA by utilizing a controlled switch in order to utilize the known power characteristics of controlled switches as a matter of obvious engineering choice” (*id.*).

Appellants argue that “Jackson . . . fails to teach or suggest [the] circuitry . . . recited in claim 1” (App. Br. 9) and that Jackson’s paragraph 26 disclosure “shows that the particular swap of a diode for a MOSFET of Jackson is not a one-size-fits all solution that a person of ordinary skill in the art would necessarily use in every situation” (*id.*).

Appellants’ argument is not persuasive because it attacks Jackson individually and does not address the combination of prior art teachings

applied in the rejection. As correctly explained by the Examiner, the test for obviousness is what the combined teachings of the applied prior art would have suggested to those of ordinary skill (Ans. 4–5). *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Further in this regard, we emphasize that Appellants do not explain how or why the paragraph 26 disclosure of Jackson is applicable to the AAPA circuit.

Appellants also contend that the circuitry of claim 1 “is not taught nor suggested in the alleged AAPA” (App. Br. 11).

As above, Appellants’ contention ineffectively is directed to AAPA alone rather than the combined teachings of AAPA and Jackson. We agree with the Examiner that these combined teachings would have suggested “applying a known technique (as disclosed in Jackson) to a known device (as disclosed in AAPA) ready for improvement to yield predictable results (replicating functionality while utilizing the known power characteristics of controlled switches, e.g. ‘without incurring the penalty of a diode voltage drop’, Jackson, paragraph [0002])” (Ans. 7–8). *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) (“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”).

For the reasons stated above and given by the Examiner, Appellants fail to show error in the rejection of claim 1 and the other independent claims on appeal.

Appellants argue that AAPA fails to teach or suggest the features of dependent claim 18 in view of the Examiner's admission that AAPA fails to disclose the controlled switch feature of parent independent claim 12 (App. Br. 16–17).

Appellants' argument lacks convincing merit. The Examiner expressly finds that AAPA teaches or would have suggested the features recited in claim 18 (Final Action 8). Appellants do not address, and therefore do not show error in, the Examiner's finding. Based on the record before us, the Examiner's proposed modification of AAPA is supported by a preponderance of evidence and would have resulted in the controlled switch of parent claim 12 as well as the features of dependent claim 18.

Finally, Appellants contest the rejection of claims 19–22 over AAPA, Jackson, and Choi by quoting the respective limitations of these claims and stating that “[u]sing an N-channel FET to connect a controller output to a level-shifter [as disclosed by Choi] fails to teach or suggest [the quoted limitation]” (App. Br. 18–22).

Appellants' statements do not show error in the rejection of claims 19–22 for the reasons given by the Examiner (Ans. 14–20) and because such statements are not substantive arguments under 37 CFR § 41.37(c)(iv) (*see In re Lovin*, 652 F.3d 1349, 1356–57 (Fed. Cir. 2011)) and are directed to Choi alone rather than the combined teachings of the applied prior art (*see In re Merck*, 800 F.2d at 1097).

The decision of the Examiner is affirmed.

Appeal 2015-006062
Application 12/097,463

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED