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EXAMINER

STEVENSON, ANDRE C

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MUNEHIRO TOYAMA,
SIEW FONG TAI, KIAN SIN SIM,
CHARAN K. GURUMURTHY and
SELVY TAMIL SELVAMUNIANDY¹

Appeal 2015-006053
Application 13/071,841
Technology Center 2800

Before BRADLEY R. GARRIS, BEVERLY A. FRANKLIN, and
MICHAEL G. MCMANUS, *Administrative Patent Judges*.

GARRIS, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Examiner's
decision rejecting claims 1–9. We have jurisdiction under 35 U.S.C. § 6.

We REVERSE.

¹ INTEL CORPORATION is identified as the real party in interest. App.
Br. 2.

Appellants claim a semiconductor chip grid array connection structure 300 comprising a metallic land grid array electrical connection surface 320, a nickel layer 312 coupled to the metallic connection surface, a palladium containing layer 314 coupled to the nickel layer, and a gold layer 316 coupled to the palladium containing layer (sole independent claim 1, Fig. 3A).

A copy of representative claim 1, taken from the Claims Appendix of the Appeal Brief, appears below.

1. A semiconductor chip grid array connection structure, comprising:
a metallic land grid array electrical connection surface;
a nickel layer coupled to the metallic connection surface;
a palladium containing layer coupled to the nickel layer; and
a gold layer coupled to the palladium containing layer.

(App Br., pg. 11, Claims Appendix.)

Under 35 U.S.C. § 103(a), the Examiner rejects as unpatentable claims 1, 2, and 4² over Mori et al. (US 5,821,627, issued Oct. 13, 1998; hereinafter “Mori”) in view of Saiki et al. (US 2005/0023033 A1, published Feb. 3, 2005; hereinafter “Saiki”) (Final Action 4–5) and rejects remaining claims 3 and 5–9 over these references in combination with additional prior art (*id.* at 5–9).

In rejecting claim 1, the Examiner expresses the following findings and conclusion regarding obviousness.

Mori fails to show, with respect to **claim #1**, a semiconductor chip grid array connection structure comprising a metallic land grid array electrical connection surface.

² Claim 4 is not listed in the statement of this rejection but nevertheless is discussed in the body thereof (Final Action 4).

Saiki teaches, with respect to **claim #1**, a semiconductor chip grid array connection comprising, a metallic (**connections; 28, 31, 32, 16, 47, 46, 48, 45**) land grid array (**item #11**) electrical connection surface (**metal facial surfaces/layers; 28, 32, 16, 47, 46**) (**page #7, paragraph 0090; page #10, paragraph 0128**).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #1**, a semiconductor chip grid array connection structure comprising a metallic land grid array electrical connection surface, into the method of Mori, as taught by Saiki, with the motivation that use of LGA's offer easier component rework, lesser chance of sideways deformation, durability and provides an unleaded electronic configuration which conforms to the future environmental standards. (*Id.* at 5–6).

Appellants argue that the Examiner has provided no reason or motivation for combining the applied references in the manner required by claim 1 (App. Br. 8–9, Reply Br. 1). For example, Appellants urge that the motivation expressed by the Examiner (i.e., “use of LGA’s [sic, LGAs] offer [sic, offers] easier component rework, lesser chance of sideways deformation, durability and provides an unleaded electronic configuration which conforms to the future environmental standards” (Final Action 5)) “appears to be a motivation to *choose* an LGA over a solder configuration, not a motivation to combine teachings between the two technologies [of Mori and Saiki]” (App. Br. 8). Similarly, Appellants urge that “neither Mori nor Saiki teach[es] any combination suggested by the Examiner, and even if combined, there is no teaching in either of the references to combine in the way that is claimed” (Reply Br. 1)

Appellants’ argument has convincing merit.

“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006), *quoted with approval in KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Here, the Examiner does not support the conclusion of obviousness with articulated reasoning and rational underpinning of meaningful specificity. As an example, the Examiner fails to identify specifically the particular metallic land grid array electrical connection surface to be combined with the structure of Mori, where the electrical connection surface would be located in Mori’s structure, or why an artisan would have provided Mori’s structure with such a connection surface at such a location. In this latter regard, we emphasize that the Examiner’s proffered motivation of LGA advantages is not supported by citation to evidence and is not embellished with any explanation why these advantages would have led an artisan to provide the structure of Mori with a metallic land grid array electrical connection surface as required by claim 1 (i.e., rather than simply replacing the structure of Mori with an LGA). These circumstances reveal that the Examiner’s obviousness conclusion regarding claim 1 is based on mere conclusory statements rather than articulated reasoning with rational underpinning.

For the above-stated reasons, we do not sustain the Examiner’s § 103 rejections of claims 1–9.

The decision of the examiner is reversed.

REVERSED