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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte BRENT S. HAUKNES,
IAN SHAEFFER, and GARY B. BRONNER

Appeal 2015-006043
Application 12/990,945
Technology Center 2100

Before JASON V. MORGAN, JOHN F. HORVATH, and
KEVIN C. TROCK, *Administrative Patent Judges*.

HORVATH, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants seek review, under 35 U.S.C. § 134(a), of the Examiner's
rejection of claims 1–75. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

SUMMARY OF THE INVENTION

The invention is directed to programming operations for memory devices using incremental programming techniques. Spec. ¶ 1.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A memory system comprising:
 - a memory device including an array of non-volatile memory cells; and
 - a memory controller having a first port to receive a program command that addresses a number of the memory cells for a programming operation, having a second port coupled to the memory device via a command pipeline, and configured to create a plurality of independent fractional program commands in response to the program command, wherein execution of each fractional program command incrementally programs the addressed memory cells with program data.

REFERENCES

Prins et al. US 2009/0172257 A1 July 2, 2009

REJECTIONS

Claims 1–75 stand rejected under 35 U.S.C. § 102(e) as anticipated by Prins. Final Act. 2.

ISSUES AND ANALYSIS

We have reviewed the Examiner’s rejection in light of Appellants’ arguments that the Examiner has erred. We disagree with Appellants’ contentions, and adopt as our own the findings and reasons set forth by the Examiner in the Final Action and the Examiner’s Answer in response to Appellants’ Appeal Brief. We highlight the following for emphasis.

Claims 1–75

Issue 1: Whether Prins discloses a plurality of independent fractional program commands

The Examiner finds Prins discloses this limitation, recited in claim 1, by disclosing dividing a single received write command into a plurality of transfer requests, “where each transfer request may invoke a plurality of page requests, and where each page request necessitate[s] a write to a plurality of pages on separate flash memory die . . . that comprise the actual flash memory cells to which the write operation is carried out.” Ans. 2 (citing Prins ¶¶ 10, 85–89, Fig. 2); Final Act. 3. The Examiner further finds that “each write to a page for a given program command may reasonably be taken as a separate fractional program command as recited in the claim,” and that Prins therefore discloses “breaking up a single host write command (program command for a same group of memory cells) into a plurality of different fractional program commands (transfer request or page requests) to carry out the write to the actual flash memory cells.” Ans. 2–3.

Appellants argue the Examiner erred because Prins’ disclosure “relates to a group of smaller ‘transfer requests’ that each handle a distinct portion of the overall data,” and “does not break up a single programming request for a same group of memory cells using a plurality of independent fractional program commands.” App. Br. 15–16.

We are not persuaded by Appellants argument. Prins discloses that when a flash memory controller receives a read or write command, it creates a “CDBinfo” data structure that specifies the Logical Block Address (LBA) range of flash memory cells to be read from or to which data is to be written. Prins ¶ 85. The controller also creates up to seven Input-Output Process

(IOP) data structures, known as transfer requests, each of which is “designed to handle a portion of the LBA range specified by the IOP.” *Id.* ¶¶ 86–87. Appellants fail to persuasively distinguish “creat[ing] a plurality of independent fractional program commands in response to [a received] program command,” as recited in claim 1, from Prins’ dividing a received read/write request into a plurality of transfer requests, each of which handles a separate address range (LBA) of the received read/write request.

Issue 2: Whether Prins discloses the execution of each fractional program command incrementally programs the addressed memory cells with program data

The Examiner finds Prins discloses this limitation, also recited in claim 1, by disclosing the “[e]xecution of each transfer request involves a plurality of independent page writes . . . to a given addressed group of memory cells,” whereby “[t]he completion of each separate page request constitutes an incremental programming of the addressed memory cells with program data.” Ans. 4 (citing Prins ¶¶ 88–89, 489, 589).

Appellants argue the Examiner erred because “[e]xecution of each of Prins’ ‘Transfer Requests’ involves a complete write or programming of the data to a given addressed group of memory cells,” and therefore, “sets in motion a complete conventional programming operation that does not employ fractional program commands.” App. Br. 16.

We are not persuaded by Appellants’ arguments. Appellants fail to persuasively distinguish the “wherein execution of each fractional program command incrementally programs the addressed memory cells with program data” recitation of claim 1 from Prins’ dividing a received write request into

multiple transfer requests, and separately executing the multiple transfer requests.

Appellants further argue that the claimed invention is distinguishable from Prins' because each of Prins' transfer requests to program individual memory cells represents a "conventional continuous sequence of PV [program/verify] cycles to the cells." Reply Br. 6. However, because Appellants raise this argument for the first time in the Reply Brief, and make no showing of good cause why it could not have been raised in the Appeal Brief, the argument is waived. *See* 37 C.F.R. § 41.41(b)(2) (2014); App. Br. 13–17; Reply Br. 4–6.

Accordingly, for the reasons discussed *supra*, we sustain the Examiner's rejection of representative claim 1, and of claims 2–75, which are not separately argued. *See* 37 C.F.R. 41.37(c)(iv) (2014); App. Br. 13.

DECISION

The Examiner's rejection of claims 1–75 under 35 U.S.C. § 102(e) as anticipated by Prins is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED