



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/616,719	09/14/2012	Simon S. CHAN	SPN06249D1C1	5514

53829 7590 10/27/2016
Cypress Semiconductor
198 Champion Court
Attention: Legal--Bldg. 6.1
San Jose, CA 95134

EXAMINER

PARKER, JOHN M

ART UNIT	PAPER NUMBER
----------	--------------

2816

MAIL DATE	DELIVERY MODE
-----------	---------------

10/27/2016

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte SIMON S. CHAN ¹

Appeal 2015-005991
Application 13/616,719
Technology Center 2800

Before BRADLEY R. GARRIS, LINDA M. GAUDETTE, and
JENNIFER R. GUPTA, *Administrative Patent Judges*.

GARRIS, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from the Examiner's decision rejecting claims 21, 23–28, 30, 31, 33–35, 37, 38, and 40–45. We have jurisdiction under 35 U.S.C. § 6.

We AFFIRM.

Appellant claims a device comprising first and second transistors 334 and interconnect 336 wherein a distance between the transistors ranges from about 1500 Å to about 10,000 Å and a width of the interconnect is approximately 40 nm to 60 nm less than the distance between the transistors

¹ Spansion LLC is identified as the real party in interest. App. Br. 3.

(independent claim 21, Figs. 3 and 6; *see also* remaining independent claims 30 and 37).

A copy of representative claim 21, taken from the Claims Appendix of the Appeal Brief, appears below.

21. A device comprising:
a source region;
a first transistor on a first side of the source region;
a second transistor on a second side of the source region; and
an interconnect,
a distance between the first transistor and the second transistor ranging from about 1500 Å to about 10000 Å,
a width of the interconnect being approximately 40 nm to 60 nm less than the distance between the first transistor and the second transistor, and
one or more of the first transistor or the second transistor including:
a first dielectric layer formed directly on a substrate associated with the source region,
a charge storage layer formed on the first dielectric layer,
a second dielectric layer formed on the charge storage layer, and
a control gate layer formed on the second dielectric layer.

The Examiner rejects claim 41 under the 2nd paragraph of 35 U.S.C. § 112 as being indefinite (Final Action 2).

Under 35 U.S.C. § 103(a), the Examiner rejects claim 21 as unpatentable over Yaegashi (US 2006/0038218 A1, published Feb. 23, 2006) in view of Lu (5,789,316, issued Aug. 4, 1998) (Final Action 3–4) and rejects the remaining claims on appeal as unpatentable over these references alone or in combination with additional prior art references (*id.* at 4–9).

Appellant presents arguments specifically directed to independent claim 21 and dependent claim 26 (App. Br. 6–9) and reiterates the claim 21 arguments in contesting the rejections of remaining independent claims 30 and 37 (*id.* at 9–13). No arguments are specifically directed to the other claims on appeal (*id.* at 6–14). Therefore, in our disposition of this appeal, we will focus on claims 21 and 26.

We sustain the rejections before us for the reasons expressed in the Final Action, the Answer, and below.

The § 112, 2nd paragraph, rejection of claim 41 is summarily sustained because Appellant does not contest it in the record of this appeal.

In the § 103 rejection of claim 21, the Examiner expresses the following conclusion of obviousness.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lu into the method of Yaegashi by forming the first and second transistors 1500-10000A apart with an interconnect being 40nm to 60nm less than the distance between the first and second transistors. The ordinary artisan would have been motivated to modify Yaegashi in the manner set forth above for at least the purpose of utilizing known processes to ensure successful device fabrication.

(Final Action 4 (citing Lu col. 7, ll. 49–59)).

In the Answer, the Examiner explains that “one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization to achieve desired transistor performance” (Ans. 2–3).

In the Appeal Brief, Appellant argues that “LU does not even mention ‘the first transistor and the second transistor,’ let alone disclose ‘a distance between the first transistor and the second transistor ranging from about

1500 Å to about 10000 Å’ and ‘a width of the interconnect being approximately 40 nm to 60 nm less than the distance between the first transistor and the second transistor,’ as recited in claim 21” (App. Br. 7–8). Similarly, in the Reply Brief, Appellant argues “LU cannot disclose or suggest ‘a width of the interconnect being approximately 40 nm to 60 nm less than the distance between the first transistor and the second transistor,’ which ‘ranges from about 1500 Å to about 10000 Å,’ since LU does not even disclose ‘a distance between the first transistor and the second transistor ranging from about 1500 Å to about 10000 Å,’ as recited in claim 21 (emphasis added)” (Reply Br. 3).

The deficiency of Appellant’s argument is the erroneous premise that Lu must expressly teach the claim limitations under review. In assessing obviousness under § 103, “the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). “The test [for obviousness] is whether the references, taken as a whole, would have suggested appellant’s invention to one of ordinary skill.” *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

The column 7 disclosure of Lu cited by the Examiner evinces that the distance between integrated circuit structures and the dimensional registration tolerance for the width of an integrated circuit feature located between two such structures are art-recognized result-effective variables. Therefore, the combined teachings of Yaegashi and Lu would have led an artisan to optimize the distance between the first and second transistors of Yaegashi as well as the dimensional tolerance for the width of Yaegashi’s interconnect in order to achieve acceptable performance as urged by the

Examiner (Ans. 2–3). We emphasize that Appellant’s reply to the Answer does not address, and therefore does not show error in, the Examiner’s optimization rationale (*see generally* Reply Brief).

Appellant also contends that the Examiner erred in finding the “mask layer” limitation of dependent claim 26 to be satisfied by element 22 in Figure 9 of Yaegashi² (App. Br. 9, *cf.* Final Action 4).

In response, the Examiner concedes that Yaegashi’s layer/film 22 is not explicitly characterized as a mask layer but determines that layer/film 22 performs the function of a mask layer and accordingly satisfies the claim 26 “mask layer” limitation when this limitation is given its broadest reasonable interpretation (Ans. 3–4). The Examiner’s determination is supported by Yaegashi’s disclosures in Figure 9 and paragraphs 137–138 which reflect that layer/film 22 necessarily participates in performance of a masking function during the etching process that forms the contact holes depicted in Figure 9.

Appellant disputes this determination by arguing that Yaegashi does not disclose any masking function performed by film 22 (Reply Br. 4). However, Appellant fails to identify any Specification disclosure that the “mask layer” of claim 26 constitutes a material or performs a function that is distinguishable from the material of Yaegashi’s film 22 and the masking function necessarily performed thereby as shown in Figure 9 and described in paragraphs 137–138 of Yaegashi. For this reason, Appellant does not

² We observe that Appellant does not present any argument regarding the corresponding mask layer limitation of independent claim 30 (*see generally* App. Br.).

Appeal 2015-005991
Application 13/616,719

reveal error in the Examiner's determination that the broadest reasonable interpretation of the claim 26 "mask layer" encompasses Yaegashi's film 22.

In summary, we sustain the Examiner § 103 rejections for the reasons given in the Final Action, the Answer, and above.

DECISION

The decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED