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EXAMINER

SCHINDLER, DAVID M

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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* KONRAD KAPSER and ARNOLD RUMP

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Appeal 2015-005938  
Application 12/619,405  
Technology Center 2800

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Before GEORGE C. BEST, N. WHITNEY WILSON, and  
DEBRA L. DENNETT, *Administrative Patent Judges*.

DENNETT, *Administrative Patent Judge*.

DECISION ON APPEAL<sup>1</sup>

STATEMENT OF THE CASE

Appellants<sup>2</sup> appeal under 35 U.S.C. § 134 from a rejection of claims 1, 3–5, 7–15, 17–20, and 23–25. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

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<sup>1</sup> In this Opinion, we refer to the Final Action mailed July 23, 2014 (“Final Act.”), the Advisory Action mailed September 8, 2014 (“Advisory Act.”), the Appeal Brief filed December 22, 2014 (“App. Br.”), the Examiner’s Answer mailed April 10, 2015 (“Ans.”), and the Reply Brief filed May 26, 2015 (“Reply Br.”).

<sup>2</sup> Appellants identify Infineon Technologies AG as the real party in interest. App. Br. 3.

The claims are directed to a method of sensing and a system including a sensor system comprising one or more comparators. Claim 1, reproduced below with the disputed limitation italicized, is illustrative of the claimed subject matter:

1. A system comprising:

a sensor circuit configured to provide a sensed signal that corresponds to a distance between the sensor circuit and an object;

comparison circuitry configured to receive an input signal that corresponds to the sensed signal and to provide output signals that switch state at different levels of the input signal to indicate different distances between the sensor circuit and the object, wherein the comparison circuitry comprises:

three hysteresis comparators, wherein the output signals comprise three output signals, with each hysteresis comparator providing one of the three output signals; and

*a logic circuit that receives the three output signals and provides two logic circuit outputs based on the three output signals, wherein the two logic circuit outputs together provide four binary logic states, wherein each of the four binary logic states indicates one of four different ranges of distances between the sensor circuit and the object.*

App. Br. 13 (Claims App'x).

## REFERENCES

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Finch	US 4,365,196	Dec. 21, 1982
Vervaeke et al. ("Vervaeke")	US 2007/0046287 A1	Mar. 1, 2007
Diener et al. ("Diener")	US 2009/0102652 A1	Apr. 23, 2009
Awizio et al. ("Awizio")	US 2009/0134865 A1	May 28, 2009
Scheller et al. ("Scheller")	US 2010/0264909 A1	Oct. 21, 2010

## REJECTIONS

Claims 1, 3, 5, 8, 15, and 17–19 stand rejected under 35 U.S.C. § 102(e) over Scheller. Final Act. 9. The claims stand rejected under 35 U.S.C. § 103(a) as follows: claims 4 and 20 over Scheller in view of Finch; claim 7 over Scheller in view of Vervaeke; and claim 9 over Scheller in view of Awizio.<sup>3</sup> *Id.* at 14 and 18–20.

## OPINION

In rejecting independent claims 1 and 18, the Examiner finds that Scheller teaches

a logic circuit that receives the three output signals and provides two logic circuit outputs based on the three output signals to indicate four different levels of the input signal, [ ] wherein each of the four binary logic states indicates one of four different ranges of distances between the sensor and the object and these

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<sup>3</sup> Appellants cancelled claims 10–13 and 23–25 in the Response After Final Action filed August 26, 2014.

logic states are based on the combination of the outputs from the comparators.

Final Act. 10. The Examiner specifically identifies Figures 3–4A of Scheller for this disclosure. *Id.*

Appellants argue that the Examiner has not met his burden of providing a reference that teaches every limitation of each allegedly anticipated claim and has not established a prima facie case of obviousness for the remaining claims. App. Br. 7. Appellants confine their arguments for patentability of all of the pending claims to distinguishing over Scheller. *See generally id.*

Appellants argue the patentability of claims 1, 3, 5, 8, 15, and 17–19 over 35 U.S.C. § 102(e) as a group. *Id.* at 9. We select independent claim 1 as representative of the claims of the group except for claims 15 and 17, which we address separately.

Appellants argue that the Examiner is wrong in asserting that “the output of logic circuit elements (272), (274), and (276) [of Scheller] can be the two outputs that are said to provide the four binary states used to indicate four distances as the output from these elements include four binary logic states and these states are used to indicate[] four different distances as seen in Figure 3B.” *Id.* at 9 (quoting Advisory Act. 2). Appellants point out that Scheller discloses a logic circuit with three outputs (elements 272, 274, and 276 of Figure 3A), whereas claim 1 requires a logic circuit with only two outputs. *Id.* at 10. The two outputs of the logic circuit of claim 1 together provide four binary logic states. *Id.* at 13 (Claims App’x).

The Examiner responds that Appellants’ use of the transitional phrase “comprising” means “the prior art can have more than what appellant is reciting.” Ans. 12. According to the Examiner, the prior art must have “at

least two logic circuit outputs used to provide four binary states,” but “nothing precludes the prior art from having more than two logic circuit outputs providing the four binary states.” *Id.*

While we agree that the transitional phrase “comprising” is open-ended, it cannot be interpreted so broadly as to vitiate the requirements of the claims. Here, claim 1 specifies that *two* logic circuit outputs together provide *four* binary logic states. App. Br. 13 (Claims App’x). At best, Scheller teaches that two logic circuit outputs (DEC1 and DEC2) provide three control signals or three logic outputs (DEC1, DEC2, and DEC3) provide four control signals. *See* Scheller Figs. 1A–1B, 3A–3B.

We agree with Appellants that the Examiner has not shown that Scheller anticipates independent claim 1. We reverse the Examiner’s rejection of claim 1 as anticipated by Scheller. Claims 3, 5, and 8 depend from claim 1; we, therefore reverse the rejection of these claims.

Because the secondary references cited by the Examiner for obviousness of claims 4, 7, and 9 do not correct the deficiencies in Scheller, the Examiner has not established a prima facie case of obviousness for these claims. We reverse the rejection of these claims.

Appellants contend that “[i]ndependent claims 15 and 18 each include limitations similar to those described above with respect to independent claim 1,” and request allowance of claims 15 and 18 for at least the same reasons. App. Br. 10.

Claim 18 recites the requirement of “providing two logic circuit outputs based on the three output signals, wherein the two logic circuit outputs together provide four binary logic states.” Therefore, we reverse the rejection of claim 18 for the same reasons provided above with respect to

claim 1. Similarly, we reverse the anticipation rejection of claim 19, which depends from claim 18. We also reverse the obviousness rejection of dependent claim 20, as the secondary reference against the claim does not correct the deficiencies in Scheller.

Claim 15, however, is another matter. We disagree with Appellants' contentions that claim 15 includes limitations similar to those described with respect to claim 1 and should be allowed for the same reasons. *See* App. Br. 10. Claim 15 is reproduced below:

15. A system comprising:
  - a sensor circuit configured to provide a sensed signal;
  - a multiplexer configured to receive three or more different threshold voltages;
  - a hysteresis comparator configured to receive the three different threshold voltages from the multiplexer and an input signal that corresponds to the sensed signal, wherein the multiplexer provides each of the three different threshold voltages to the hysteresis comparator over a period of time and the hysteresis comparator compares the input signal to each of the three different threshold voltages and provides an output signal for each comparison of the input signal to one of the three different threshold voltages during the period of time; and
  - a logic circuit to receive the output signal for each comparison of the input signal to one of the three different threshold voltages during the period of time and provide binary logic states that indicate four different levels of the input signal.

App. Br. 14 (Claims App'x).

Unlike independent claims 1 and 18, claim 15 does not require that two outputs of the logic circuit together provide four binary logic states, thus Appellants' arguments on this issue are inapplicable to claim 15. *See* Ans.

14. Claim 17 depends from claim 15 and further requires an amplifier

Appeal 2015-005938  
Application 12/619,405

configured to receive the sensed signal and provide the input signal. App. Br. 15 (Claims App'x). Appellants raise no other arguments for patentability of claims 15 or 17 over Scheller.

On the record before us, the Examiner did not err in rejecting claims 15 and 17 as anticipated by Scheller.

#### DECISION

For the above reasons, the Examiner's rejection of claims 1, 3–5, 7–9, and 18–20 is reversed, and rejection of claims 15 and 17 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART