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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* TORU KAMBAYASHI, TAKU KATO,  
HIROSHI SUKEGAWA, YOSHIHIKO HIROSE, and  
KOICHI FUJISAKI

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Appeal 2015-005792  
Application 12/880,513  
Technology Center 2400

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Before DEBRA K. STEPHENS, KEVIN C. TROCK, and  
JESSICA C. KAISER, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION ON APPEAL

*Introduction*

Appellants<sup>1</sup> appeal under 35 U.S.C. § 134(a) from a final rejection of claims 2 and 4.<sup>2</sup> We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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<sup>1</sup> According to Appellants, the real party in interest is Kabushiki Kaisha Toshiba (App. Br. 1).

<sup>2</sup> Claims 1, 5, and 6 have been cancelled. (App. Br. 20, 22). The Examiner has stated that claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. (Final Act. 11).

EXEMPLARY CLAIM

Claim 2, reproduced below, is illustrative of the claimed subject matter with disputed limitations emphasized:

2. An information storing system in which *a reading device and a writing device are connected to a memory chip, wherein the memory chip comprises:*

*a memory including a second area that is common area to which writing is performed and from which reading is performed, the memory including a first area, the first area including the second area, the first area being an area to which data is written by the writing device that is authenticated by the memory chip;*

the writing device comprises:

a first encryption key generating circuit that receives first key information stored in the memory and generates a first key by processing the first key information, the first key being used to encrypt data stored in the writing device; and

a data transmitter that transmits, to the memory chip, first encrypted data obtained by encrypting the data using the first key, and

the memory chip further comprises:

a converting circuit that receives the first encrypted data and converts the first encrypted data by using a second key, the second key being paired with the first key stored in the writing device, and the second key being used to decrypt the first encrypted data;

a writing circuit that writes the data that is converted, in the first area;

*a second encryption key generating circuit that receives second key information stored in the reading device and generates a third key by processing the second key information, the third key being used to encrypt data stored in the second area; and*

*a transmitter that transmits second encrypted data to the reading device, the second encrypted data being data that is obtained by encrypting data stored in the second area using the third key, and*

the reading device receives the second encrypted data and decrypts the second encrypted data by using a fourth key, the fourth key being paired with the third key stored in the memory chip and the fourth key being used to decrypt the second encrypted data.

### REJECTION

The Examiner made the following rejection:

Claims 2 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tatebayashi (US 7,298,845 B2; issued Nov. 20, 2007), Chambers (US 2010/0077230 A1; published Mar. 25, 2010), and Yanagisawa (US 2005/0027993 A1; published Feb. 3, 2005). (Final Act. 5–11).

### ISSUES

*Issue 1a:* Did the Examiner err in finding the combination of Tatebayashi and Yanagisawa teaches or suggests recited components being arranged on “a single memory chip,” as Appellants contend is required by claim 2 and similarly required by claim 4?

*Issue 1b:* Did the Examiner err in finding Tatebayashi teaches or suggests “a reading device and a writing device are connected to a memory chip,” as recited in claim 2 and similarly recited in claim 4?

*Issue 1c:* Did the Examiner err in finding the combination of Tatebayashi and Chambers teaches or suggests

the memory chip comprises: a memory including a second area that is common area to which writing is performed and from which reading is performed, the memory including a first area, the first area including the second area, the first area being an area to which data is written by the writing device that is authenticated by the memory chip,

as recited in claim 2 and similarly recited in claim 4?

*Issue 1d:* Did the Examiner err in finding the combination of Tatebayashi and Yanagisawa teaches or suggests “a second encryption key generating circuit that receives second key information stored in the reading device and generates a third key by processing the second key information, the third key being used to encrypt data stored in the second area,” as recited in claim 2 and similarly recited in claim 4?

*Issue 1e:* Did the Examiner err in finding Tatebayashi teaches or suggests “a transmitter that transmits second encrypted data to the reading device, the second encrypted data being data that is obtained by encrypting data stored in the second area using the third key,” as recited in claim 2 and similarly recited in claim 4?

*Issue 1f:* Did the Examiner err in finding Tatebayashi, Chambers, and Yanagisawa teaches or suggests “a converting circuit” and “a writing circuit,” as recited in claim 2 and similarly recited in claim 4?

*Issue 2:* Did the Examiner improperly combine Tatebayashi, Chambers, and Yanagisawa?

## ANALYSIS

We have reviewed the Examiner’s rejections and the evidence of record in light of Appellants’ argument that the Examiner has erred. We disagree with Appellants’ arguments and conclusions. We adopt as our own

the findings and reasons set forth by the Examiner in the action from which this appeal is taken (Final Act. 5–11 (mailed May 28, 2014)), the findings and reasons set forth by the Advisory Action (Adv. Act. 2 (mailed Sept. 24, 2014)) and the findings and the reasons set forth in the Examiner’s Answer (Ans. 3–21 (mailed March 20, 2015)). We concur with the conclusions reached by the Examiner and further highlight specific findings and argument for emphasis as follows.

*Issue 1a*

Appellants argue<sup>3</sup> Yanagisawa does not teach that its components are arranged on a single memory chip as required by claims 2 and 4. (App. Br. 10–11; Reply Br. 3–6). In particular, Appellants argue the claims “require[ ] that the second encryption key generating circuit and the transmitter be part of the memory chip that also includes a memory having the claimed first and second memory areas.” (Reply Br. 3–4 (emphasis omitted)). In other words, according to Appellants, the recited “memory” must contain the recited “first and second memory areas” as well as the “second encryption key generating circuit” and the “transmitter.” Appellants contend the Examiner errs in finding Yanagisawa teaches such a single memory chip because Yanagisawa’s “DVD disc 18 and the transmitting device 19 . . . are each separate, standalone devices and are not arranged or configured on a single memory chip.” (App. Br. 10 (emphasis omitted); *see* Reply Br. 5).

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<sup>3</sup> To the extent Appellants’ summarization of the Examiner’s Final Office Action, which discusses limitations the Examiner “admitted” were not taught by an individual reference, contains an argument (App. Br. 7–9), we note that the Examiner relies on Chambers and Yanagisawa to address Tatebayashi’s “admitted” deficiencies (Final Act. 6–10).

We are not persuaded. Appellants’ argument is unpersuasive because the Examiner does not rely on Yanagisawa alone to teach the recited components, but rather relies on the combination of Tatebayashi and Yanagisawa. (Ans. 4–5; Final Act. 6, 8–9). In addition, Appellants’ argument does not persuasively address the Examiner’s finding that it is “within the scope of knowledge and skills of [ ] one skill[ed] in [the] art to combine different units on a single chip” (Ans. 14–15), and therefore, an ordinarily skilled artisan would have found it obvious to incorporate the data encryption and transmission features taught by Yanagisawa into Tatebayashi’s single memory chip to “us[e] key information from a receiving device to generate an encryption key, which is used to encrypt data to be transmitted to the receiving device” (Final Act. 9).

We are also unpersuaded by Appellants’ argument that “the Examiner is selectively ignoring [Yanagisawa’s] DVD 18, and merely picking out the functionality of the data transmitter 11 and the transmission side data processor 13, and stating that it would have been obvious to also put those elements on the chip disclosed by [Tatebayashi]” (Reply Br. 3, 5; *see* App. Br. 10) because the Examiner does not rely on a bodily incorporation of Yanagisawa’s structure into the structure of Tatebayashi. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007); *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Instead, the Examiner relies on teachings from Yanagisawa (e.g., its use of a key to encrypt data to be sent from a transmitting device to a reading device (Final Act. 8–9 (citing Yanagisawa ¶¶ 24, 41); Ans. 4 (citing Yanagisawa ¶ 34, Fig. 3)) and finds an ordinarily skilled artisan would have found it obvious to apply those teachings to Tatebayashi’s memory card that transmits data to a memory card reader (Final Act. 6

(citing Tatebayashi Fig. 1), 9–10; Ans. 3 (citing Tatebayashi 11:20–24, 66–67, 12:1–8, Fig. 4)).

Accordingly, we are not persuaded the Examiner erred in finding the combination of Tatebayashi and Yanagisawa teaches or suggests recited components being arranged on “a single memory chip,” as Appellants contend is required by claim 2 and similarly required by claim 4.

*Issue 1b*

Appellants argue Yanagisawa does not teach “a reading device and a writing device are connected to a memory chip,” as recited in claim 2 and similarly recited in claim 4. (App. Br. 11). Specifically, Appellants argue, without further elaboration, Yanagisawa does not teach that its “DVD disc 18 is a memory chip connected to a reading device and a writing device.” (*Id.* at 11 (emphasis omitted)). Appellants further argue, without elaboration, Yanagisawa’s “transmission side processing device 31” is not “connected to a ‘writing device.’” (*Id.*).

We are not persuaded because Appellants’ arguments are not responsive to the Examiner’s rejection, which relies on Tatebayashi, not Yanagisawa, to teach “a reading device and a writing device are connected to a memory chip.” Specifically, the Examiner finds, and we agree, Tatebayashi teaches memory card 200 which transmits data with memory card reader 400 and memory card writer 300 (Final Act. 6 (citing Tatebayashi 8:55–63, Figs. 1, 4); Ans. 3 (citing Tatebayashi 11:20–24, 66–67, 12:1–8, Fig. 4); *see also* Tatebayashi 8:37–50).

Accordingly, we are not persuaded the Examiner erred in finding Tatebayashi teaches “a reading device and a writing device are connected to a memory chip,” within the meaning of claims 2 and 4.

*Issue 1c*

Appellants argue Yanagisawa does not teach the memory chip comprises: a memory including a second area that is common area to which writing is performed and from which reading is performed, the memory including a first area, the first area including the second area, the first area being an area to which data is written by the writing device that is authenticated by the memory chip, as recited in claim 2 and similarly recited in claim 4. (App. Br. 10, 12; *see* Reply Br. 4). Specifically, Appellants argue, without further elaboration, Yanagisawa does not teach that its “DVD disc 18 [is] on a second area that is a common area of the writing and reading areas and including a first area that includes a second area into which data writing is performed by the writing unit authenticated by the DVD disc 18.” (App. Br. 10 (emphasis omitted); *see* Reply Br. 4). Moreover, Appellants argue Yanagisawa does not teach “that data writing is performed with respect to the DVD disc 18 by the writing unit authenticated by the DVD disc 18.” (App. Br. 12 (emphasis omitted)).

We are not persuaded because the Examiner relies on the combination of Tatebayashi and Chambers, not Yanagisawa, as teaching the disputed limitation. (Final Act. 6–8). Specifically, the Examiner finds, and we agree, Tatebayashi’s memory card includes a “a second area (e.g., [ ] storing unit 210 or 220) that is a predetermined data storage area (e.g., [ ] storing unit 220 is predetermined to store media inherent key) and the memory card also

includes a first area (e.g.,] storing unit 260).” (Final Act. 6 (citing Tatebayashi 8:55–63, Fig. 4)). The Examiner further finds, and we agree, Chambers teaches a memory chip with a protected memory field 42 “to which writing and read is performed,” i.e., a second area, that is included within a programmable memory 24 area, i.e., a first area. (*Id.* at 7–8 (citing Chambers ¶¶ 31, 36, 44–48, Figs. 1–2)). The Examiner applies Chamber’s teaching that a first area includes a second area to Tatebayashi’s memory card’s first area and second area. (*Id.* at 8).

Accordingly, we are not persuaded the Examiner erred in finding Tatebayashi teaches

the memory chip comprises: a memory including a second area that is common area to which writing is performed and from which reading is performed, the memory including a first area, the first area including the second area, the first area being an area to which data is written by the writing device that is authenticated by the memory chip,  
within the meaning of claims 2 and 4.

#### *Issue 1d*

Appellants argue Yanagisawa does not teach “a second encryption key generating circuit that receives second key information stored in the reading device and generates a third key by processing the second key information, the third key being used to encrypt data stored in the second area,” as recited in claim 2 and similarly recited in claim 4. (App. Br. 10–11). Specifically, Appellants argue, without further elaboration, Yanagisawa’s “DVD disc 18” does not teach this limitation. (*Id.* at 10 (emphasis omitted); *see id.* at 11).

We are not persuaded because Appellants' argument attacks Yanagisawa individually whereas the Examiner relies on the combination of Tatebayashi and Yanagisawa as teaching this limitation. In particular, the Examiner finds, and we agree, Tatebayashi's memory chip provides encryption by "receiv[ing] the key information B<sub>j</sub> from the memory card reader 400 and generat[ing] the apparatus key A'<sub>j</sub> by processing the received key information B<sub>j</sub>." (Ans. 4 (citing Tatebayashi 11:43–48, 12:9–36)). Further, the Examiner finds, and we agree, Yanagisawa teaches a system which uses an encryption key to encrypt data transmitted to a receiving device. (Final Act. 8–9 (citing Yanagisawa ¶ 34, Fig. 3); Ans. 4). The Examiner finds an ordinarily skilled artisan would have found it obvious to incorporate the data encryption and transmission features taught by Yanagisawa into Tatebayashi's memory chip to "us[e] key information from a receiving device to generate an encryption key, which is used to encrypt data to be transmitted to the receiving device" (Final Act. 9).

Appellants' argument is unpersuasive because it attacks Yanagisawa individually (App. Br. 10), rather than persuasively addressing the Examiner's combination of references, i.e., Tatebayashi and Yanagisawa. *In re Keller*, 642 F.2d at 426. Accordingly, we are not persuaded the Examiner erred in finding the combination of Tatebayashi and Yanagisawa teaches "a second encryption key generating circuit that receives second key information stored in the reading device and generates a third key by processing the second key information, the third key being used to encrypt data stored in the second area," within the meaning of claims 2 and 4.

*Issue 1e*

Appellants argue Yanagisawa does not teach “a transmitter that transmits second encrypted data to the reading device, the second encrypted data being data that is obtained by encrypting data stored in the second area using the third key,” as recited in claim 2 and similarly recited in claim 4. (App. Br. 10; *see* App. Br. 11–12). Specifically, Appellants argue, without further elaboration, Yanagisawa’s “DVD disc 18 does not have a transmitter” and “fails to disclose a memory chip that includes a transmitter.” (App. Br. 10 (emphasis omitted); *see* App. Br. 11–12).

We are not persuaded because the Examiner relies on the combination of Tatebayashi and Yanagisawa to teach a memory chip with a transmitter which transmits encrypted data to a reading device (Ans. 8–9; Final Act. 9–10). In particular, the Examiner finds, and we agree Tatebayashi teaches a memory card which transmits encrypted data with a memory card reader and a memory card writer (Ans. 3 (citing Tatebayashi 11:20–24, 66–67, 12:1–8, Fig. 4); Final Act. 6 (citing Tatebayashi Figs, 29, 31)). The Examiner further finds, and we agree, Yanagisawa also teaches data transmitter 11, not DVD disc 18, transmits encrypted data to a receiving unit. (Final Act. 8–9 (citing Yanagisawa ¶ 34, Fig. 3)).

Appellants’ arguments do not persuasively address the Examiner’s findings regarding Tatebayashi’s memory card or Yanagisawa’s data transmitter. Accordingly, we are not persuaded the Examiner erred in finding Tatebayashi teaches “a transmitter that transmits second encrypted data to the reading device, the second encrypted data being data that is obtained by encrypting data stored in the second area using the third key,” within the meaning of claim 2 and claim 4.

*Issue 1f*

Appellants, for the first time in the Reply Brief, raise the arguments that Tatebayashi “fails to disclose the converting circuit” (Reply Br. 6), Chambers “fails to disclose the claimed converting circuit and the claimed writing circuit” (*id.* at 6–7 (emphasis omitted)), and Yanagisawa does not teach “the claimed converting circuit and the claimed writing circuit” (*id.* at 7). These arguments are waived because they were not initially presented in the opening brief and were not in response to a new argument presented by the Examiner. *Optivus Tech., Inc. v. Ion Beam Applications S.A.*, 469 F.3d 978, 989 (Fed. Cir. 2006) (argument raised for the first time in the reply brief that could have been raised in the opening brief is waived); *accord Ex parte Borden*, 93 USPQ2d 1473, 1473–74 (BPAI 2010) (informative) (absent a showing of good cause, the Board is not required to address an argument newly presented in the reply brief that could have been presented in the principal brief on appeal).

Furthermore, even considering these arguments, we find these unpersuasive because they attack the references individually, rather than addressing the combination of references on which the Examiner relies. More specifically, Appellants argue Tatebayashi and Yanagisawa do not teach a converting circuit (Reply Br. 6–7), but the Examiner relies on Chambers to teach a converting circuit (Final Act. 7–8 (citing Chambers ¶¶ 15, 18, 24–25, 27, Fig. 1)). Additionally, Appellants argue Yanagisawa does not teach a writing circuit (Reply Br. 7); however, the Examiner relies on Chambers to teach the writing circuit (Final Act. 8 (citing Chambers ¶¶ 31, 366, 44–48, Figs. 1–2)). Moreover, Appellants argue Chambers does not disclose the converting circuit and the writing circuit because Chambers

does not teach a received encryption key (Reply Br. 6), but the Examiner relies on Tatebayashi to teach a received encryption key (Final Act. 6 (citing Tatebayashi 13:55–47, 14:1–3, 9–10, 42:23–30, 40–43, Figs. 29, 31)).

Thus, even considering Appellants’ untimely arguments regarding the claimed “converting circuit” and “writing circuit,” we are not persuaded of Examiner error.

### *Issue 2*

Appellants argue the Examiner improperly combined Tatebayashi, Chambers, and Yanagisawa. Specifically, Appellants argue “there is no disclosure in [Yanagisawa] that would serve as motivation to combine the memory unit 14 disclosed by [Chambers] with the DVD disc 18 disclosed by [Yanagisawa].” (App. Br. 12.) Appellants further argue the combination is “unfeasible” because “there is no motivation for applying the function of generating a third key from the information received from a reader (e.g., [Yanagisawa’s] transmission side control data processor 13) and the function of transmitting data that is encrypted with the third key (e.g., [Yanagisawa’s] data transmitter 11) to [Tatebayashi’s] memory card.” (Reply Br. 5–6 (emphasis omitted)).

We are not persuaded. The Examiner finds, and we agree, Tatebayashi teaches the “combination of different units, all implemented on a single chip.” (Ans. 14). The Examiner concludes an ordinarily skilled artisan would have found it obvious to combine Tatebayashi, Chambers, and Yanagisawa to “provide[ ] a convenient way to generate a pair of symmetric key[s] in a secure data communication system” for “encryption [of data] at

the transmitter device and decryption [of data] at the receiving device” (Final Act. 9–10).

Appellants’ argument that “there is no in disclosure in [Yanagisawa] that would serve as motivation to combine” (App. Br. 12) is unpersuasive because the Examiner’s reason for combining references need not come from the references themselves. *See KSR*, 550 U.S. at 419 (“The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents.”). Appellants have not persuaded us of error in the Examiner’s conclusion that an ordinarily skilled artisan would have found it obvious for Tatebayashi’s memory card to use a key to encrypt and send data to a reading device because the Examiner’s reasoning for the modification is supported by rational underpinning—providing a manner of generating symmetric keys for secure data transfer (Final Act. 9–10). Furthermore, Appellants’ argument that the combination is “unfeasible” because “there is no motivation” for the combination (*see* Reply Br. 5–6) does not address the Examiner’s stated motivation for the combination, and Appellants do not explain how the purported lack of motivation for combining references makes the combination “unfeasible.” Moreover, Appellants’ unfeasibility arguments are supported only by attorney argument, which is not evidence. *In re Pearson*, 494 F.2d 1399, 1405 (CCPA 1974) (“Attorney’s argument in a brief cannot take the place of evidence.”). Accordingly, we are not persuaded the Examiner improperly combined Tatebayashi, Chambers, and Yanagisawa.

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DECISION

The Examiner's rejection of claims 2 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Tatebayashi, Chambers, and Yanagisawa is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED