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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte KOJI KUROKI

Appeal 2015-005509
Application 13/137,252
Technology Center 2800

Before BRADLEY R. GARRIS, JULIA HEANEY, and
JEFFREY R. SNAY, *Administrative Patent Judges*.

HEANEY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant¹ seeks our review pursuant to 35 U.S.C. § 134(a) of a decision of the Examiner to reject claims 1–10 and 21 of Application 13/137,252. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

BACKGROUND

The subject matter on appeal relates to a semiconductor device comprising signal wiring and dummy wiring. App. Br. 2–3. According to Appellant’s Specification, first signal wirings may be provided as bit lines,

¹ Appellant identifies the real party in interest as PS4 Luxco S.a.r.l. App. Br. 1.

all of which are supplied with substantially the same electrical potential. Spec. p. 11, ll. 16–17; p. 14, ll. 15–18. The objective of this feature is to provide higher reliability than conventional devices in which all bit lines are not in the same electrical potential environment. Spec. p. 14, ll. 19–21; App. Br. 3.

Claim 1 is representative of the claimed subject matter:

1. A semiconductor device comprising:
 - a first signal wiring configured to be supplied with a first signal potential;
 - a first dummy wiring insulated from the first signal wiring, the first dummy wiring being configured to be supplied with a fixed potential; and
 - a second dummy wiring between the first signal wiring and the first dummy wiring, the second dummy wiring being insulated from the first dummy wiring, the second dummy wiring being configured to be supplied with substantially the same potential as the first signal potential.

App. Br. 23, Claims Appx.

THE REJECTIONS

1. Claims 1, 7, and 21 are rejected under 35 U.S.C. § 102(b) as anticipated by Kaneda.²
2. Claims 2–6 and 8–10 are rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Kaneda and Kanda.³

DISCUSSION

Anticipation Rejection

² Kaneda US 7,675,784 B2 Mar. 9, 2010 (hereinafter “Kaneda”).

³ Kanda US 7,428,161 B2 Sep. 23, 2008.

Appellant argues that Kaneda does not anticipate claim 1 because it does not disclose a “first dummy wiring being configured to be supplied with a fixed potential” or a “second dummy wiring being configured to be supplied with substantially the same potential as the first signal potential.” App. Br. 9–14.

The Examiner finds that Kaneda’s first dummy bit line **DBL1** (Fig. 1) corresponds to the first dummy wiring recited in claim 1, and that **DBL1** is supplied with a fixed potential, $\frac{1}{2} V_{cc}$, during the bit line discharge period (Fig. 2). Final Act. 4–5. Appellant argues that the potential of Kaneda’s **DBL1** is not fixed because it varies from 0 to $\frac{1}{2} V_{cc}$ during a bit line charge period. App. Br. 12–13, citing Kaneda Fig. 2. Appellant further argues that the Examiner’s selection of the bit line discharge period as the window during which **DBL1** is fixed is arbitrary, and thus unreasonable, because there is no reason to select that period over the bit line charge period, during which the potential of **DBL1** changes from 0 to $\frac{1}{2} V_{cc}$. *Id.*

As to the second dummy wiring, the Examiner finds Kaneda’s second dummy bit line **DBL2** corresponds to the second dummy wiring recited in claim 1, and that **DBL2** is supplied with substantially the same potential as bit line **BL** during the bit line charge period. i.e., V_{cc} . Final Act. 5, citing Kaneda Figs. 1–2. Appellant disputes the Examiner’s finding and argues that the potential of **DBL2** in fact remains unchanged at V_{cc} during bit line charge, while **BL** changes from 0V to V_{cc} , and further that the potential of **DBL2** is reduced from V_{cc} to $\frac{1}{2} V_{cc}$ during bit line discharge, while **BL** drops from V_{cc} to 0V. App. Br. 13, citing Kaneda Fig. 2. Appellant further argues that the Examiner’s selection of the bit line charge period as the window during which **DBL2** is at V_{cc} is arbitrary because there is no reason to select that period over the bit line charge period. App. Br. 14.

Appellant's arguments are persuasive of harmful error in the Examiner's findings as to the potential of Kaneda's **DBL1** and **DBL2**. For the reasons stated by Appellant and discussed above, we determine that the Examiner's findings that Kaneda's **DBL1** temporarily is supplied with a fixed potential, and **DBL2** momentarily is supplied with a potential substantially the same as **BL**, do not support a finding of anticipation.

Because we find reversible error in the rejection of claim 1, and the Examiner's rejection of the dependent claims does not remedy the errors identified above, we likewise reverse the anticipation rejection of claims 7 and 21.

Obviousness Rejection

The obviousness rejection is directed only to claims which depend from claim 1, and is based on the same findings with respect to Kaneda as the anticipation rejection. Because we find reversible error in those findings, we also reverse the rejection of claims 2–6 and 8–10 under 35 U.S.C. § 103(a) as unpatentable over the combination of Kaneda and Kanda.

SUMMARY

We reverse the rejection of claims 1, 7, and 21 under 35 U.S.C. § 102(b) as anticipated by Kaneda.

We reverse the rejection of claims 2–6 and 8–10 under 35 U.S.C. § 103(a) as unpatentable over the combination of Kaneda and Kanda.

REVERSED