UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/926,415	11/16/2010	James Nolan Hardage	SCS-550-1314	9788

73459 7590 11/02/2016
NIXON & VANDERHYE, P.C.
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER
GIROUX, GEORGE

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
11/02/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOMAIL@nixonvan.com
pair_nixon@firsttofile.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JAMES NOLAN HARDAGE,
GLEN ANDREW HARRIS, and MARK CARPENTER GLASS

Appeal 2015-005109
Application 12/926,415
Technology Center 2100

Before ELENI MANTIS MERCADER, CARL L. SILVERMAN, and STEVEN M. AMUNDSON, *Administrative Patent Judges*.

AMUNDSON, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants[1] seek our review under 35 U.S.C. § 134(a) from a final rejection of claims 1, 2, 4–12, and 14–19, i.e., all pending claims. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

---

[1] According to Appellants, the real party in interest is ARM Limited. App. Br. 4.

STATEMENT OF THE CASE

The Invention

According to the Specification, the "invention relates to buffer stores for use within data processing systems." Spec. 2:6–7.[2] A buffer includes a main store and an auxiliary store that hold micro-operation instructions, and "[r]ead control circuitry serves to control reading . . . such that target addresses are read from the auxiliary store in association with the predicted taken branch instructions read from the main store." Abstract.

Representative Claim

Independent claim 1 exemplifies the subject matter of the claims under consideration and reads as follows, with italics identifying the limitations at issue in claim 1:

> 1. A buffer store comprising:
>
> main store circuitry configured to store N main values to be read in a predetermined main sequence;
>
> auxiliary store circuitry configured to store M auxiliary values, M being less than N and each auxiliary value of said M auxiliary values being associated with a main value of said N main values; and
>
> read control circuitry configured to control reading from said main store and from said auxiliary store such that *said auxiliary value is read from said auxiliary store in association with said main value*, *wherein said read control circuitry is configured to detect from said main value read from said main*

[2] This decision uses the following abbreviations: "Spec." for the Specification, filed November 16, 2010; "Non-Final Act." for the Non-Final Office Action, mailed June 20, 2013; "Amend." for the Amendment, filed September 23, 2013; "Final Act." for the Final Office Action, mailed October 4, 2013; "App. Br." for the Appeal Brief, filed June 24, 2014; "Ans." for the Examiner's Answer, mailed February 12, 2015; and "Reply Br." for the Reply Brief, filed April 13, 2015.

> *store circuitry that said main value is associated with said auxiliary value and to trigger said auxiliary value to be read from said auxiliary store circuitry.*

App. Br. 26 (Claims App.).

The Prior Art Supporting the Rejections on Appeal

The Examiner cites the following prior art:

Favor et al. ("Favor")	US 6,453,278 B1	Sept. 17, 2002
Tran et al. ("Tran")	US 2004/0186985 A1	Sept. 23, 2004

The Rejections on Appeal

Claims 1, 2, 4–8, 10–12, and 14–18 stand rejected under 35 U.S.C. § 102(b) as anticipated by Favor. Final Act. 4–7.

Claims 9 and 19 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Favor. Final Act. 8.

ANALYSIS

We have reviewed the rejections of claims 1, 2, 4–12, and 14–19 in light of Appellants' arguments that the Examiner erred. For the reasons explained below, we disagree with Appellants' assertions regarding error by the Examiner.

The Rejection of Claims 1, 10, and 11 Under 35 U.S.C. § 102(b)

Appellants argue that independent claims 1, 10, and 11 require serial operation, i.e., that "the 'main value' (from said main store circuitry) must **first** be read out from the main store, **second** is examined to 'detect' whether that 'main value' is 'associated with said auxiliary value' and **third**, only if that detection is made, then triggers the 'auxiliary value to be read from said auxiliary store circuitry.'" App. Br. 10–11; *see id.* at 12, 15–16, 17, 21; Reply Br. 2–3, 5. Appellants seek to distinguish the claims from Favor by

asserting that (1) Favor discloses accessing a "main store" in parallel with accessing an "auxiliary store" using the same address to index both stores and (2) "Favor requires advance notice of the 'association' between the main store and the auxiliary store." App. Br. 10; *see id.* at 21; Reply Br. 3.

The Examiner finds that Favor teaches that (1) an instruction cache (i.e., main store) receives instruction data, (2) a predecode stage adds predecode data to the instruction data, (3) an instruction buffer (i.e., also main store) stores the instruction and predecode data, (4) an instruction decoder employing short decoders and a branch history table (BHT) determines from the instruction and predecode data in the instruction buffer (i.e., main store) if a branch is predicted taken, and (5) if a branch is predicted taken, the circuitry reads a target value from a branch target buffer (i.e., auxiliary store). Ans. 2–3, 4–5, 5–6; *see* Final Act. 4, 8–9. Thus, the Examiner determines that the circuitry first reads a value in an instruction buffer (i.e., main store), second detects an association between the read value and a target value in a branch target buffer by decoding the read value, and third reads the target value in the branch target buffer to branch when appropriate.

When addressing these findings, Appellants admit that "there can be an association between a main value read from a main store and an auxiliary value read from an auxiliary store in Favor." Reply Br. 4; *see* App. Br. 13. But Appellants assert that the "association is not detected 'from said main value read from said main store circuitry,' as required by the independent claims." Reply Br. 4–5; *see* App. Br. 13. That assertion rests on Appellants' contention that Favor uses the same address to index the instruction cache

(main store) and the branch target buffer (auxiliary store). Reply Br. 3, 5 (citing Favor 23:60–24:22, Fig. 2, Fig. 4).

But the portions of Favor that Appellants cite do not state that the circuitry reads values from the main store and the auxiliary store in parallel using the same address. Instead, those portions explain that if a short decoder in an instruction decoder determines that a branch is predicted taken, the circuitry changes the value in the instruction cache (main store) to a value immediately following the target value in the branch target buffer (auxiliary store) and the changed value in the instruction cache together with predecode data then loads into the instruction buffer (auxiliary store). Favor 23:66–24:13. Based in part on the portions of Favor that Appellants cite, the Examiner instead finds that an instruction decoder determines from the data in the instruction buffer (i.e., main store) if a branch is predicted taken, and if a branch is predicted taken, the circuitry reads a target value from a branch target buffer (i.e., auxiliary store). *See*, *e.g.*, Ans. 2–3 (citing Favor 6:15–25, 6:33–55, 7:1–25, 7:44–8:11, 23:54–24:48, Fig. 2, Fig. 4).

Appellants contend that the Examiner does not indicate where Favor discloses any configuration "to detect from said main value read from said main store circuitry that said main value is associated with said auxiliary value." App. Br. 13–14, 15, 20–21. As explained above, however, the Examiner finds that Favor teaches an instruction decoder employing short decoders and a branch history table (BHT) to determine from the instruction and predecode data in the instruction buffer (main store) if a branch is predicted taken. Ans. 2–3, 4–5, 5–6; *see* Final Act. 4, 8–9. Hence, Favor teaches detecting from a value read from a main store an association with an auxiliary value.

Appellants also contend that the Examiner does not indicate where Favor discloses triggering "said auxiliary value to be read from said auxiliary store circuitry" based on the value read from the main store. App. Br. 15–16, 21. As explained above, however, the Examiner finds that Favor teaches that if a branch is predicted taken based on the instruction and predecode data in the instruction buffer (main store), the circuitry reads a target value from the branch target buffer (auxiliary store). Ans. 2–3, 4–5, 5–6; *see* Final Act. 4, 8–9. Hence, Favor teaches triggering the reading of an auxiliary value from an auxiliary store based on a value read from a main store.

Appellants attempt to distinguish Favor based on operation in the event of "some problem in the set-up" or "corruption" in the data. App. Br. 14; Reply Br. 5. But the Examiner's findings regarding Favor rest on normal operation, not abnormal operation. *See* Ans. 2–3, 4–5, 5–6; *see also* Final Act. 4, 8–9.

Based on the word "possibly" in the Examiner's statement that "Favor *does* teach serial access of instruction cache followed (possibly) by [branch target buffer] BTB access," Appellants assert that "the rejection is speculative rather than factual." Reply Br. 3; *see* Ans. 3. As we understand that statement, however, it refers to the typical linear processing of instructions through the instruction cache and the instruction buffer with the branch target buffer used intermittently ("possibly") to branch when appropriate.

Accordingly, Appellants' arguments have not persuaded us that the Examiner erred in rejecting claims 1, 10, and 11 as anticipated by Favor. Hence, we sustain the rejection.

The Rejection of Claims 2, 4–8, 12, and 14–18 Under 35 U.S.C. § 102(b)

Claims 2 and 4–8 depend directly or indirectly from claim 1, while claims 12 and 14–18 depend directly or indirectly from claim 11. App. Br. 26–27, 29–30 (Claims App.). Appellants do not present any separate patentability arguments for these dependent claims. App. Br. 10–21; Reply Br. 1–6. Because Appellants do not argue these dependent claims separately, we sustain the rejection of the dependent claims for the reasons applicable to the independent claims. *See* 37 C.F.R. § 41.37(c)(1)(iv).

The Rejection of Claims 9 and 19 Under 35 U.S.C. § 103(a)

Claim 9 depends from claim 1, while claim 19 depends from claim 11. App. Br. 27, 30 (Claims App.). Claims 9 and 19 specify that "N is greater than 10*M," i.e., a main store size greater than 10 times an auxiliary store size. *Id.* at 27, 30.

In the Non-Final Office Action, the Examiner took "official notice that it would have been an obvious matter of design choice to choose a value wherein N is greater than 10*M, since such a modification would have involved only a choice of an optimal size, or changing the size of the component . . . ." Non-Final Act. 8.

In response, Appellants challenged the Examiner's reliance on official notice because (1) Favor "contains no such disclosure" and (2) Appellants are "unaware of any prior art which teaches such a disclosure." Amend. 9. Appellants requested that the Examiner provide evidence supporting the official notice. *Id.*

In the Final Office Action, the Examiner disputed that Appellants adequately traversed the official notice due to a failure to explain "why the noticed fact is not considered to be common knowledge or well-known in

the art." Final Act. 9–10 (quoting *MPEP* § 2144.03(C)). In addition, the Examiner repeated the rationale that "it would have been an obvious matter of design choice" to achieve the claimed subject matter. *Id.* at 8.

In the Appeal Brief, Appellants again challenged the Examiner's reliance on official notice, e.g., as "merely a conclusory statement." App. Br. 18–19, 21–24. Appellants again requested that the Examiner provide evidence supporting the official notice, e.g., to meet the "burden of proof with respect to a *prima facie* case of obviousness." *Id.* at 23.

In the Answer, the Examiner maintains that Appellants did not adequately traverse the official notice. Ans. 7. Nevertheless, the Examiner identifies Tran as supporting the official notice. *Id.* at 8. The Examiner finds that "Tran teaches that the size of the [branch target buffer] BTB may be based upon the size of the instruction cache, and that the instruction cache is 32 times as large as the [branch target buffer] BTB," i.e., 32K for the main store versus 1K for the auxiliary store. *Id.* (citing Tran ¶ 35). The Examiner also finds that "Favor teaches that the size of the [branch target buffer] BTB should remain small, in order to reduce complexity" and that "Favor and Tran are analogous art, as they are within the same field of endeavor, namely instruction processing." *Id.* (citing Favor 24:36–48).

In the Reply Brief, Appellants note that the Examiner did not designate the Favor-Tran combination as a new ground of rejection and that the Answer presents a new issue regarding claims 9 and 19. Reply Br. 6. Appellants contend that the citation to Tran in the Answer "is improper" and that "it is too late for the Examiner to now supply a reference for the purported 'official notice' position." *Id.* But Appellants do not dispute the Examiner's findings regarding Favor or Tran. *Id.*

Insofar as Appellants protest a failure to designate a new ground of rejection, they present their protest to an inappropriate entity. The *Manual of Patent Examining Procedure* (*MPEP*) explains that 37 C.F.R. § 41.40 provides the "exclusive procedure" for requesting review of a failure to designate a new ground of rejection, i.e., through a petition to the Director under 37 C.F.R. § 1.181. *MPEP* § 1207.03(b) (9th ed. Rev. 07.2015 Nov. 2015). The *MPEP* also explains that "[t]his procedure should be used if an appellant feels an answer includes a new ground of rejection that has not been designated as such and wishes to reopen prosecution . . . ." *Id.*

Appellants apparently have not submitted a petition to the Director. The "[f]ailure of [an] appellant to timely file such a petition will constitute a waiver of any arguments that a rejection must be designated as a new ground of rejection." 37 C.F.R. § 41.40(a).

We agree with the Examiner that Tran teaches a main store size greater than 10 times an auxiliary store size. *See* Tran ¶ 35. We also agree with the Examiner that Favor teaches an auxiliary store with a relatively small size, e.g., compared to a main store. *See* Favor 24:45–48; *see also* Final Act. 8.

Design choices that do not "result in a difference in function or give unexpected results . . . are no more than obvious variations consistent with the principles known in that art." *In re Rice*, 341 F.2d 309, 314 (CCPA 1965). Appellants do not argue that appropriately sizing a main store vis-à-vis an auxiliary store results in a difference in function or gives unexpected results. App. Br. 18–19, 21–24; Reply Br. 6. "If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

Accordingly, we discern no error in the Examiner's obviousness analysis for claims 9 and 19 in the Final Office Action. As for Tran, it provides the support for the official notice that Appellants repeatedly requested.

Thus, Appellants' arguments have not persuaded us that the Examiner erred in rejecting claims 9 and 19 for obviousness. Hence, we sustain the rejection.

DECISION

We affirm the Examiner's decision to reject claims 1, 2, 4–12, and 14–19.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED