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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DAVID T. WANG, SURESH NATARAJAN RAJAN, KEITH R. SCHAKEL, MICHAEL JOHN SEBASTIAN SMITH, and FREDERICK DANIEL WEBER

Appeal 2015-004751
Application 11/672,924
Technology Center 2100

Before MARC S. HOFF, JAMES R. HUGHES, and
TERRENCE W. McMILLIN, *Administrative Patent Judges*.

HUGHES, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants seek our review under 35 U.S.C. § 134(a) of the Examiner’s Final Decision rejecting claims 21, 24–29, 31–34, and 44, which constitute all the claims pending in this application. *See* App. Br. 2.¹ We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

¹ We refer to Appellants’ Specification (“Spec.”) (filed Feb. 8, 2007) (claiming benefit of US 60/772,414 (filed Feb. 9, 2006) and US 60/865,624 (filed Nov. 13, 2006)); Appeal Brief (“App. Br.”) (filed Oct. 17, 2014); and Reply Brief (“Reply Br.”) (filed Mar. 18, 2015). We also refer to the Examiner’s Answer (“Ans.”) (mailed Feb. 20, 2015), and Final Office Action (Final Rejection) (“Final Act.”) (mailed May 8, 2014).

Appellants' Invention

The invention at issue on appeal concerns apparatuses, systems and methods for controlling memory, in particular, simulating (virtualizing) memory circuits and associating the virtual memory circuits with a set of scheduling constraints. (Spec. ¶¶ 2, 4; Abstract.)

Illustrative Claim

Independent claim 21, reproduced below with the key disputed limitations emphasized, further illustrates the invention:

21. An apparatus comprising:

an interface circuit electrically connected to a first number of physical dynamic random access memory (“DRAM”) devices via multiple data paths including a first data path and a distinct second data path, wherein each of the physical DRAM devices is an individual and independent monolithic device, the interface circuit configured to:

communicate with the first number of physical DRAM devices and a memory controller,

interface the first number of physical DRAM devices to simulate a different, second number of virtual DRAM devices, such that the first number of physical DRAM devices appear to the memory controller as the second number of virtual DRAM devices, each of the virtual DRAM devices being simulated as an individual and independent monolithic device,

simulate a first virtual DRAM device using a first physical DRAM device on the first data path and a second physical DRAM device on the distinct second data path,

use both a physical row of the first physical DRAM device and a physical row of the second physical DRAM device to simulate a virtual row of the first virtual DRAM device,

receive a row-access command from the memory controller, directed to the first virtual DRAM device, for the virtual row of the first virtual DRAM device,

receive a column-access command from the memory controller, directed to the first virtual DRAM device, for a particular column of the virtual row, wherein the column-access command from the memory controller is received before the row-access command is used to activate any physical DRAM device,

based on the received column-access command, translate the row-access command for the virtual row to a row-access command for either the physical row of the first physical DRAM device or the physical row of the second physical DRAM device that corresponds to part of the virtual row, and

activate either the physical row of the first physical DRAM device or the physical row of the second physical DRAM device based on the translated row-access command to activate only part of the virtual row.

Rejection on Appeal

The Examiner rejects claims 21, 24–29, 31–41, and 44 under 35 U.S.C. § 103(a) as being unpatentable over Ruckerbauer et al. (US 2006/0129740 A1; published June 15, 2006 (filed Dec. 13, 2004)) (“Ruckerbauer”), Lee et al. (US 6,262,938 B1, issued July 17, 2001) (“Lee”), and Manton et al. (US 4,500,958, issued Feb. 19, 1985) (“Manton”)

RELATED APPEAL

Appellants indicate that an Appeal Brief was filed for a related patent application, U.S. Patent Application No. 11/672,921, January 24, 2014. App. Br. 1. The appeal has been assigned Appeal No. 2014-006763. The Board has not issued a decision on Appeal No. 2014-006763. Appellants

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indicate that an Appeal Brief was filed for a related patent application, U.S. Patent Application No. 11/929,225, January 24, 2014. App. Br. 1. The appeal has been assigned Appeal No. 2014-006782. The Board has not issued a decision on Appeal No. 2014-006782. Appellants indicate that an Appeal Brief was filed for a related patent application, U.S. Patent Application No. 13/620,650, May 27, 2014. App. Br. 1. The appeal has been assigned Appeal No. 2015-001955. The Board has not issued a decision on Appeal No. 2015-001955.

ISSUE

Based upon our review of the administrative record, Appellants' contentions, and the Examiner's findings and conclusions, the pivotal issue before us is as follows:

Does the Examiner err in finding that the combination of Ruckerbauer, Lee, and Manton collectively would have taught or suggested "an interface circuit configured to" "interface the first number of physical DRAM devices to simulate a different, second number of virtual DRAM devices," within the meaning of Appellants' claim 21 and the commensurate limitations of claims 31 and 36?

ANALYSIS

Appellants contend that Ruckerbauer does not teach the disputed limitation of claim 21 because Ruckerbauer does not describe an interface circuit configured to interface a number of physical DRAM devices to simulate a different, second number of virtual DRAM devices. *See* App. Br. 11–17; Reply Br. 1–7. Specifically Appellants contend that Ruckerbauer

contains “no disclosure of a virtual memory device or of virtualization of memory devices.” App. Br. 13.

Appellants persuade us of error in the obviousness rejection of claim 21. We have reviewed the sections of Ruckerbauer cited by the Examiner. While Ruckerbauer generally describes multiple independent memory devices sharing a data bus (*see* Final Act. 3–5; Ans. 2–7 (citing Ruckerbauer ¶¶ 9, 27, 39, 41; Fig. 1), which the Examiner maintains meets Appellants’ virtualization limitation (*supra*), we agree with Appellants that the Examiner does not establish these sections disclose simulating memory circuits (i.e., virtual memory). Appellants’ claim requires an interface not only capable of simulating memory (memory circuits), but simulating a first group (number) of memory circuits as second group of memory circuits having a different number of memory circuits. The Examiner has not shown that Ruckerbauer describes virtual (simulated) memory, much less the specific simulation recited in claim 21.

Consequently, we are constrained by the record before us to find that the Examiner erred in finding Ruckerbauer, Lee, and Manton teach the disputed limitations of Appellants’ claim 21. Independent claim 31 includes limitations of commensurate scope. Claims 24–29, 32–41, and 44 depend on claims 21, 31 and 36, respectively. Accordingly, we reverse the Examiner’s obviousness rejection of claims 21, 24–29, 31–41, and 44.

CONCLUSION

Appellants have shown that the Examiner erred in rejecting claims 21, 24–29, 31–41, and 44 under 35 U.S.C. § 103(a).

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DECISION

We reverse the Examiner's rejection of claims 21, 24–29, 31–41, and
44.

REVERSED