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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JI-SOO PARK and JAMES G. FIORENZA

Appeal 2015-004492
Application 12/562,206
Technology Center 2800

Before PETER F. KRATZ, ROMULO H. DELMENDO, and DONNA M. PRAISS, *Administrative Patent Judges*.

PRAISS, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

STATEMENT OF CASE

Appellants[2] appeal under 35 U.S.C. § 134 from the Examiner's decision to reject claims 1–10 and 21–30 under 35 U.S.C. § 103(a) as follows:

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[1] In this decision, we refer to the Specification filed September 18, 2009 (Spec.), the Final Office Action appealed from mailed March 7, 2014 (Final Act.), the Appeal Brief filed September 25, October 20, 2014 (App. Br.), the Examiner's Answer mailed January 5, 2015 (Ans.), and the Reply Brief filed March 5, 2015 (Reply Br.).

[2] The real party in interest is identified by Appellants as Taiwan Semiconductor Manufacturing Company, Ltd. by assignment from AmberWave Systems. App. Br. 2.

1. Claims 1, 2, 4, 5, 7, 8, 10, 21, 22, 24, 26, 27, 29, and 30 over Lochtefeld '667[3] and Lochtefeld '126;[4]
2. Claims 3, 23, and 28 over Lochtefeld '667, Lochtefeld '126, and Levy;[5]
3. Claims 6 and 25 over Lochtefeld '667, Lochtefeld '126, and Bai;[6] and
4. Claim 9 over Lochtefeld '667, Lochtefeld '126, and Chen.[7]

We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

The claims are directed to a semiconductor device. Claims 1, 21, and 26 are independent. Claim 1 is illustrative (subject matter in dispute italicized):

> 1. A semiconductor device, comprising:
>
> a composite structure comprising a first semiconductor crystalline material in an opening of a second material, the opening having an aspect ratio sufficient to trap a majority of defects, the composite structure having a planar surface; and
>
> a second semiconductor crystalline material over the first semiconductor crystalline material at the planar surface, the second semiconductor crystalline material comprises a strain, *wherein a top surface of the first semiconductor crystalline material has a surface roughness RMS of 5 nm or less, and*

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[3] Lochtefeld, US 2008/0073667 A1, published Mar. 27, 2008 ("Lochtefeld '667").
[4] Lochtefeld et al., US 2006/0197126 A1, published Sept. 7, 2006 ("Lochtefeld '126").
[5] Levy et al., US 2009/0110898 A1, published Apr. 30, 2009 ("Levy").
[6] Bai et al., US 2008/0099785 A1, published May 1, 2008 ("Bai").
[7] Chen et al., US 2005/0148161 A1, published July 7, 2005 ("Chen").

> *wherein an interface between the first and second semiconductor crystalline materials has a reduced impurity concentration.*

Claims App'x to App. Br. 1.

Appellants do not separately argue the patentability of the claims. App. Br. 5–11. In accordance with 37 C.F.R. § 41.37(c)(1)(iv), and based upon the lack of arguments directed to the subsidiary rejections, claims 2–10 and 21–30 will stand or fall together with claim 1.

OPINION

Regarding claim 1, the Examiner finds that Lochtefeld '667 discloses all of the elements of the claimed semiconductor device with the exception of the requirement that the top surface of the first semiconductor crystalline material has a surface roughness RMS of 5 nm or less, and wherein an interface between the first and second semiconductor crystalline materials has a reduced impurity concentration. Final Act. 3 (citing Lochtefeld '667 ¶¶ 40, 42–46, Fig. 4). The Examiner also finds that Lochtefeld '126 teaches a reduced impurity concentration between the first and second semiconductor crystalline materials (*id.* (citing Lochtefeld '126 ¶ 132, Fig. 39)) and, specifically, "a low surface roughness (i.e. 5 nm or less, specifically 0.5 nm [0071]), which achieves the advantage of providing epitaxial layers with minimized surface rough, providing greater surface area which enhances the quality of bonding in the structure" (*id.* at 4 (citing Lochtefeld '126 ¶¶ 67, 68, 71)). The Examiner concludes that it would have been obvious to one having ordinary skill at the time of the invention to modify Lochtefeld '667 with the teachings of Lochtefeld '126 "to provide a top surface of the first semiconductor crystalline material [with] a surface roughness RMS of 5 nm or less, in order to achieve greater surface area, enhancing the quality of subsequent bonding." *Id.*

Appellants contend that the Examiner's rejection of claim 1 is in error because paragraph 71 of Lochtefeld '126 achieves the disclosed surface roughness by chemical mechanical polishing (CMP) and "one of skill would not apply a CMP to the semiconductor material S2 [of Lochtefeld '667] because doing so would destroy the structure taught by Lochtefeld '667." App. Br. 7. Appellants assert that the Examiner's rejection is conclusory because "[t]he Examiner provides no explanation of how a CMP can be applied to the second semiconductor material S2 consistent with the teachings of Lochtefeld '667." *Id.* at 8. Because Lochtefeld '667's semiconductor materials S2 and S3 form an interface within a trench defined by dielectric material, Appellants contend that contacting the semiconductor material S2 with a polishing pad to planarize the surface would remove all of the dielectric material above that surface in the CMP process and destroy the purpose of the structure of Lochtefeld '667. *Id.* at 9. Additionally, Appellants assert that the Examiner's combination of Lochtefeld '667 and Lochtefeld '126 lacks a rational underpinning because Lochtefeld '126 planarizes "to improve a quality of the subsequent wafer bond" while "Lochtefeld '667 has nothing to do with wafer bonding . . . ." *Id.* at 10.

The Examiner responds that "the claims neither require nor preclude [a] CMP process." Ans. 4. Regarding obtaining the surface roughness taught by Lochtefeld '126 in the device of Lochtefeld '667, the Examiner further finds:

> Although it may be difficult to have an RMS roughness of less than 0.5 nm using CMP in the structure of Lochtefeld (667) as applicant Appellant alleges, it is not impossible [to] achieve. Other forms of surface processing for example, ion etching could be used in the structure of Lochtefeld (667) to achieve the desired RMS roughness.

Id. The Examiner also finds that Lochtefeld '667 teaches a first semiconductor crystalline material (S2) and the second semiconductor crystalline material (S3) "over the first semiconductor crystalline." *Id.* at 3.

In the Reply Brief, Appellants argue that "[w]ithout some technical explanation, the Examiner's statement that 'it is not impossible' is speculation and a conclusory generalization that is insufficient to support a prima facie case of obviousness." Reply Br. 2–3. Regarding other forms of surface processing such as ion etching, Appellants continue to assert that this is conclusory, not technical reasoning by the Examiner and otherwise provide no substantive rebuttal. *Id.* at 3. Regarding bonding between semiconductor materials S2 and S3 in Lochtefeld '667, Appellants assert that "a low surface roughness for wafer bonding are not present with epitaxial bonds formed during epitaxial growth." *Id.* at 5.

We are not persuaded by Appellants' arguments and find that the preponderance of the evidence supports the rejection of claim 1 for the reasons provided by the Examiner in the Final Action and the Answer. Final Act. 3–4; Ans. 2–4. We add the following for emphasis.

Appellants' arguments are unpersuasive because the Examiner's finding that Lochtefeld '126 teaches a reduced impurity concentration at the interface of crystalline semiconductor material that improves device performance is supported. Lochtefeld '126 ¶ 132. We are not persuaded that Lochtefeld '667 crystalline layers S2 and S3 do not have a bond at their interface or that Lochtefeld '667 has nothing to do with wafer bonding. *See* Lochtefeld '667 ¶¶ 35 ("[t]he crystalline material 140 may be formed by selective epitaxial growth in any suitable epitaxial deposition system"), 36 ("[t]he epitaxial growth system may be a single-wafer or multiple-wafer

batch reactor."), 47, Fig. 4. We also are not persuaded that the Examiner erred in finding that it would have been obvious to enhance the quality of subsequent bonding and achieve greater surface area by planarizing the first crystalline layer of Lochtefeld '667 as taught by Lochtefeld '126. Based on the record before us, planarizing of the first crystalline layer is not limited to any particular method by the cited references. *See, e.g.*, Lochtefeld '126 ¶¶ 67 ("planarization may be performed by a method such as chemical mechanical polishing (CMP)"), ¶ 71 ("planarized by, e.g., CMP"); *see also* Lochtefeld '667 ¶ 53 ("planarized by, e.g., chemical-mechanical polishing (CMP)"). Appellants do not explain adequately why ion etching would be an insufficient means for planarizing a crystalline layer or why at least a portion of the surface of crystalline layer S2 would not be amenable to being planarized by chemical mechanical polishing. *See* Reply Br. 2–4.

In sum, Appellants have not persuaded us of reversible error in the Examiner's finding that the teaching of Lochtefeld '126 to improve interface quality with a low RMS of less than 0.5 nm for subsequent bonding would have been an obvious modification to improve the quality of the interface between the first and second crystalline semiconductor materials of Lochtefeld '667.

CONCLUSION

We sustain the Examiner's rejections.

DECISION

The Examiner's decision is affirmed.

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

AFFIRMED