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LARKIN HOFFMAN DALY & LINDGREN, LTD.
8300 Norman Center Drive
Suite 1000
Minneapolis, MN 55437

EXAMINER
SHEDRICK, CHARLES TERRELL

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JON M. HUPPENTHAL, THOMAS R. SEEMAN,
JEFFREY HAMMES, and D. JAMES GUZY

Appeal 2015-004338
Application 13/365,090
Technology Center 2600

Before CARLA M. KRIVAK, MICHAEL J. STRAUSS, and
NABEEL U. KHAN, *Administrative Patent Judges*.

STRAUSS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1–56. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

THE INVENTION

The claims are directed to mobile electronic devices utilizing reconfigurable processing techniques to enable higher speed applications with lowered power consumption. Spec., Title. Claim 1, reproduced below, is representative of the claimed subject matter:

> 1. A mobile device comprising:
> reconfigurable logic;
> a memory system coupled to said reconfigurable logic; and
> microprocessor logic also coupled to said memory system, wherein said reconfigurable logic and said microprocessor logic are peers with respect to access to said memory system.

REFERENCES

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Lewis	US 2004/0018853 A1	Jan. 29, 2004
Burton	US 7,424,552 B2	Sept. 9, 2008

REJECTIONS

The Examiner made the following rejections:

Claims 1–3, 8, 9, 17–19, 24, 25, 33–35, 40, 41, 48 and 50 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lewis and Burton. Final Act. 7–9.

Claims 4–7, 10–16, 20–23, 26–32, 36–39, 42–47, 49 and 51–56 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lewis, Burton, and Appellants' Admitted Prior Art (AAPA). Final Act. 9.

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' arguments the Examiner has erred. We disagree with Appellants' conclusions. We adopt as our own (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken (Final Act. 2–9) and (2) the reasons set forth by the Examiner in the Examiner's Answer in response to Appellants' Appeal Brief (Ans. 2–7) and concur with the conclusions reached by the Examiner. We highlight the following for emphasis. We consider Appellants' arguments *seriatim*, as they are presented in the Appeal Brief, pages 7–13.

Appellants contend Lewis "does not disclose, teach or suggest the use of reconfigurable computing for processing smart phone applications, to reduce application processing power consumption or to increase application process computational capability." Br. 7. Such argument is unpersuasive of error because, as found by the Examiner, the argued features are not recited in the claims. Ans. 2. *See also In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (limitations not appearing in the claims cannot be relied upon for patentability).

Appellants next contend "<u>the processor 506 and modulator/demodulator 504 of Lewis are not peers with respect to access to the caching mechanism 506</u>" and, therefore, fail to disclose the disputed limitation "wherein said reconfigurable logic and said microprocessor logic

are peers with respect to access to said memory system" as required by claim 1. Br. 7. This contention is unpersuasive because it attacks an inapposite reference with respect to the argued feature and fails to address the Examiner's finding that Burton's disclosure of both reconfigurable logic and microprocessor logic coupled to, and peers with respect to accessing, a memory system teaches or suggests the disputed limitation. Final Act. 8, Ans. 2–3. As explained by the Examiner (*id.*), "[n]on-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Appellants further contend the combination of Lewis and Burton applied in rejecting claim 1 is improper because (i) Burton and Lewis are directed to non-analogous art (Br. 10–11); (ii) the Examiner has failed to articulate reasoning with sufficient rational underpinning to support the legal conclusion of obviousness (*id.*); and (iii) modifying Lewis's cache 506 to provide access by *both* demodulator 504 and processor 505 as taught by Burton would render cache 506 unsatisfactory for its intended purpose and/or change its principle of operation. Br. 11–12.

We disagree for the reasons set forth by the Examiner. Ans. 3–7. Furthermore, in connection with contention (i), we note, although Appellants contend the cited references are not amongst themselves analogous art (i.e., "the shared memory resources of Burton are in no way analogous to the caching mechanism of Lewis" (Br. 12)), "[i]n order for a reference to be proper for use in an obviousness rejection under 35 U.S.C. § 103, the reference must be analogous art *to the claimed invention*." Memorandum

from Robert W. Bahr to the Patent Examining Corps 1 (July 26, 2011), *available at* http://www.uspto.gov/patents/law/exam/analogous_art.pdf (citing *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004)) (emphasis added). In particular, to be considered in an obviousness analysis, the art must be analogous "prior art," which means the prior art must be in either the same field of Appellants' endeavor or reasonably pertinent to Appellants' problem. *In re Clay*, 966 F.2d 656, 659 (Fed. Cir. 1992). Whether a prior art reference is "analogous" is a question of fact. *Id.* at 658. Appellants fail to provide sufficient evidence or argument that neither Lewis or Burton is (i) from the same field of endeavor nor (ii) reasonably pertinent to Appellants' problem to persuade us of Examiner error. Instead, as found by the Examiner, both references are directed to microprocessor logic coupled to a memory system and, therefore, are at least from the same field of endeavor as Appellants' claimed device including reconfigurable and microprocessor logic devices coupled to a common memory system. Ans. 3. Accordingly, both Lewis and Burton are analogous art to the claimed invention.

We also disagree the Examiner has failed to articulate reasoning with sufficient rational underpinning to support the legal conclusion of obviousness. Br. 10–11. The Examiner finds one skilled in the art would have provided peer access to a memory system to improve performance by reducing system latency as disclosed by Burton. Final Act. 8, Ans. 3–4. In the absence of sufficient rebuttal evidence or reasoning, we find the Examiner's reasoning sufficient to support the legal conclusion of obviousness.

In response to contention (iii) arguing Lewis's device would be rendered inoperative or its principle of operation changed if modified

according to Burton, the Examiner finds "the Applicant is suggesting one of many possible manners of combining and why the one of many combinations may be flawed." Ans. 6. We agree. As explained by the Examiner, "Applicant's argument appears to be based on an attempt to make the cache of Lewis analogous with the memory of the claimed invention" rather than considering Lewis for what it would have taught or suggested, i.e., a memory system in general that could, but need not, be implemented as a cache mechanism. *Id.* That is, not only are Appellants' arguments speculative and unsubstantiated, it is well settled that "a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (citations omitted). Nor is the test for obviousness whether a secondary reference's features can be bodily incorporated into the structure of the primary reference. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Therefore, Appellants' contention (iii) is unpersuasive of Examiner error.

For the reasons discussed *supra*, we are unpersuaded of Examiner error. Accordingly, we sustain the rejections of independent claim 1 and, for the same reasons, independent claims 17, 33, and 50 under 35 U.S.C. § 103(a) together with the rejections of dependent claims 2–16, 18–32, 34–49, and 51–56, which are not argued separately.

DECISION

We affirm the Examiner's decision to reject claims 1–56.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED