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SLATER MATSIL, LLP 17950 PRESTON ROAD SUITE 1000 DALLAS, TX 75252			LEE, HSIEN MING	
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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte OSKAR NEUHOFF, TOBIAS GAMON,
NORBERT MARTIN HAUEIS, DIRK PIKORZ,
MICHAEL WOLFGANG LARISCH, and
FRANZ REITHNER

Appeal 2015-003795
Application 13/558,299
Technology Center 2800

Before ADRIENE LEPIANE HANLON, TERRY J. OWENS, and
BRIAN D. RANGE, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

The Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1–5, 21, and 22. We have jurisdiction under 35 U.S.C. § 6(b).

The Invention

The Appellants claim a system and method for producing a device including a semiconductor part and a non-semiconductor part. Claim 1 is illustrative:

1. A system for producing a device that include [sic, includes] a semiconductor part and a non-semiconductor part, the system comprising:
 - a front end configured to receive the semiconductor part and to process the semiconductor part;
 - a back end configured to receive the processed semiconductor part and to assemble the processed semiconductor part and the non-semiconductor part into the device; and
 - a transfer device configured to automatically handle the semiconductor part in the front end and to automatically transfer the processed semiconductor part to the back end.

The References

Haris	US 2006/0056952 A1	Mar. 16, 2006
Chung	US 2008/0278188 A1	Nov. 13, 2008

The Rejections

Claims 1–5, 21, and 22 stand rejected under 35 U.S.C. § 103 over Chung in view of Haris.

OPINION

We reverse the rejection. We need address only the independent claims (1, 21, and 22).

Chung discloses (¶ 3):

Generally, a process for manufacturing a semiconductor is largely divided into a front-end process and a back-end process. The front-end process, which is a fabrication process, is a process for forming an integrated circuit pattern on a wafer. The back-end process, which is an assembly process, is a process for forming an integrated circuit package by dividing the wafer into a plurality of chips, connecting a conductive lead or ball to each chip so as to provide electrical path or external devices and then molding the chips with epoxy, etc.

Haris discloses a semiconductor processing apparatus (8) which “may be any desired processing tool, such as a semiconductor workpiece generation/formation tool (capable of carrying out any desired semiconductor formation process such as layer-growing process or material deposition, lithography and etching, cleaning, baking, polishing), stocker or metrology tool” (¶ 17; Fig. 2). The apparatus (8) comprises a front section (30) which may be an environmental front end module (EFEM) including a sorting device (10), and a back section (31) which may include one or more processing stations and, if desired, a workpiece transport system for carrying out one or more of the above-listed processes or any other desired combination of processing (¶ 17). “[T]he back section **31** may interface with EFEM **30** via one or more load locks” (*id.*).

The Examiner asserts (Ans. 4–5):

[Haris’s] “front end module 30” and “back section 31” are equivalent to “front end” and “back end, respectively, in the claimed invention because both the front end module 30 and back section 31 in Haris have similar corresponding functionalities to “front end” and “back end” as in the present claims. In particular, Haris teaches that the front end module 30 is “configured to receive the semiconductor part and to process the semiconductor part”, e.g. to receive the workpiece or semiconductor wafers W from the carrier 40 via load port module 50 (Fig. 2, Haris) and to process the semiconductor wafers W, such as to deposit, etch and/or clean the wafers W (para [0017], lines 7-13, Haris).

Haris’s front section (30) does not process workpieces but, rather, moves workpieces between transport carriers (40) and one or more buffer modules (20) (and optional aligners (32)) (¶¶ 17–20; Fig. 2). The workpiece processing is carried out in the back section (31) (¶ 17). Thus, Haris’s back

section (31) corresponds to the Appellants' front end. The Examiner does not establish that the applied prior art discloses or would have suggested, to one of ordinary skill in the art, a device or step for automatically transferring a processed workpiece from the back section (31) to another section capable of assembling it and another part into a device. Nor does the Examiner establish that Haris's automatic transfer of workpieces from the front section (30) to the workpiece-processing back section (31) (¶ 17) would have suggested automatically transferring workpieces between semiconductor processing apparatus sections generally, such as from a workpiece-processing section to an assembly section (Chung ¶ 3).

Thus, the Examiner has not set forth a factual basis which is sufficient to support a prima facie case of obviousness of the Appellants' claimed invention. *See In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967) ("A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art"). Accordingly, we reverse the rejection.

DECISION/ORDER

The rejection of claims 1–5, 21, and 22 under 35 U.S.C. § 103 over Chung in view of Haris is reversed.

It is ordered that the Examiner's decision is reversed.

REVERSED