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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* ISRAEL CIDON, AVINOAM KOLODNY, and  
WALTER ZIGMOND ISASK'HAR<sup>1</sup>

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Appeal 2015-003183  
Application 12/745,711  
Technology Center 2100

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Before MAHSHID D. SAADAT, NORMAN H. BEAMER, and  
JAMES W. DEJMEK, *Administrative Patent Judges*.

DEJMEK, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 1–29. Claims 30 and 31 are objected to as being dependent upon a rejected base claim, but would otherwise be allowable if rewritten in independent form. Final Act. 21. We have jurisdiction over the remaining pending claims under 35 U.S.C. § 6(b).

We affirm.

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<sup>1</sup> Appellants identify Technion R&D Foundation Ltd. as the real party in interest. Br. 3.

## STATEMENT OF THE CASE

### *Introduction*

Appellants' claimed invention is directed to a bus enhanced network on chip ("BENoC"). Spec. ¶ 11. According to the Specification, communication between various modules within an integrated circuit may be accomplished via either a bus or network. Spec. ¶¶ 19–22. In a disclosed embodiment, a network and bus are arranged in parallel such that communication of critical signals is performed over the bus, which has a lower latency as compared to the network. Spec. ¶ 24. Further according to the Specification, the network on chip provides a high performance distributed network and allows for benefits of network communication performance (e.g., lower power and size requirements, greater throughput, and scalability) for non-time-critical communications. Spec. ¶¶ 3, 6, 19, 20.

Claim 1 is representative of the subject matter on appeal and is reproduced below:

1. A system comprising:  
multiple modules of an integrated circuit;  
a network on chip that is coupled to the multiple modules;  
and  
a bus, coupled in parallel to the network on chip to at least two modules of the multiple modules; wherein a latency of the bus is lower and more predictable than a latency of the network of chip.

### *The Examiner's Rejections*

1. Claims 1–8, 15–21, 28, and 29 stand rejected under 35 U.S.C. § 102(a) as being anticipated by David Ilitzky et al., *Architecture of the*

*Scalable Communication Core's Network on Chip*, IEEE MICRO, Sept.–Oct. 2007, 62–74 (IEEE Computer Soc'y) (“Iltzky”). Final Act. 5–8.

2. Claims 9 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iltzky. Final Act. 9.

3. Claims 10–14 and 23–27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iltzky and Salvador Coll et al., *Scalable Hardware-Based Multicast Trees*, 1–21 (ACM 2003) (“Coll”). Final Act. 9–12.

4. Claims 1–7, 9, 15–19, 20, 22, 28, and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kang et al. (US 2005/0271054 A1; Dec. 8, 2005) (“Kang”) and Tufford et al. (US 2006/0062227 A1; Mar. 23, 2006) (“Tufford”). Final Act. 12–17.

5. Claims 8, 10–14, and 23–27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kang, Tufford, and Coll. Final Act. 17–21.

#### *Issues on Appeal*

1. Did the Examiner err in relying on Iltzky as being prior art to Appellants' claimed invention?

2. Did the Examiner err in finding “wherein the bus is arranged to wake up units of the network on chip,” as recited in claim 9, obvious over Iltzky and the knowledge of a person having ordinary skill in the art?

3. Did the Examiner err in finding Iltzky discloses “wherein the bus conveys time-critical point to point data transactions and the network on chip conveys non time-critical point to point data transactions,” as recited in claim 28?

4. Did the Examiner err in finding the combination of Kang and Tufford teaches or suggests “a bus, coupled in parallel to the network on chip,” as recited in claim 1?

5. Did the Examiner err in finding the combination of Kang and Tufford teaches or suggests “wherein the bus conveys time-critical point to point data transactions and the network on chip conveys non time-critical point to point data transactions,” as recited in claim 28?

## ANALYSIS<sup>2</sup>

### *Rejection of claims 1–8 and 15–21 under 35 U.S.C. § 102(a)*

Appellants contend the Examiner erred in relying on Iltzky in rejecting, *inter alia*, independent claims 1 and 15 because Iltzky does not qualify as prior art to Appellants’ invention. Br. 8–9. In particular, Appellants assert Iltzky was published in the September/October 2007 of *Micro, IEEE* (Volume: 27, Issue: 5), whereas the claimed subject matter of the pending claims was “reduced to practice . . . well before” the Iltzky article was published. Br. 8. In support of this assertion, Appellants submit a declaration of Mr. Kolodny stating an early draft of a Ph.D. research proposal, dated June 27, 2007, disclosed the elements of the claimed invention. Declaration of A. Kolodny, dated August 18, 2013 (“Kolodny Decl.”). Additionally, Appellants state work on the claimed invention was published in a December 2007 article entitled “BENoC: A Bus-Enhanced Network on-Chip. Br. 8 (attached as Exhibit I to Appellants’ Appeal Brief).

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<sup>2</sup> Throughout this Decision, we have considered the Appeal Brief, filed October 7, 2014 (“Br.”); the Examiner’s Answer, mailed on October 23, 2014 (“Ans.”); and the Final Office Action (“Final Act.”), mailed on February 7, 2014, from which this Appeal is taken.

Appellants argue the Ph.D. proposal, the continuation of work related to the claimed invention, the December 2007 publication of the bus-enhanced network on chip article, and the filing of a provisional patent application on December 6, 2007 evidence “a reduction to practice that was followed by due diligence.” Br. 8–9.

Title 37 of the Code of Federal Regulations, § 1.131(b) states:

(b) The showing of facts [] shall be such, in character and weight, as to establish reduction to practice prior to the effective date of the reference, or conception of the invention prior to the effective date of the reference coupled with due diligence from prior to said date to a subsequent reduction to practice or to the filing of the application. Original exhibits of drawings or records, or photocopies thereof, must accompany and form part of the affidavit or declaration or their absence must be satisfactorily explained.

Where conception occurs prior to the date of the reference, but reduction to practice is afterward, it is not enough merely to allege that the applicant had been diligent. *Ex parte Hunter*, 1889 C.D. 218, 49 O.G. 733 (Comm’r Pat. 1889). Rather, applicants must show evidence of facts establishing diligence. The actual dates of acts relied on to establish diligence must be provided. *See also MPEP* §§ 715.07 (II), 715.07 (a) and 2138.06 regarding the diligence requirement.

To establish due diligence, an applicant must account for the entire period during which diligence is required. The affidavit or declaration and exhibits must clearly explain which facts or data applicant is relying on to show completion of his or her invention prior to the particular date. Vague and general statements in broad terms about what the exhibits describe along with a general assertion that the exhibits describe a reduction to practice “amounts essentially to mere pleading, unsupported by proof or a showing

of facts” and, thus, does not satisfy the requirements of 37 C.F.R. § 1.131(b). *In re Borkowski*, 505 F.2d 713 (CCPA 1974); *In re Harry*, 333 F.2d 920, 923 (CCPA 1964) (statement that the subject matter “was diligently reduced to practice” is not a showing but a mere pleading); *Kendall v. Searles*, 173 F.2d 986, 993 (CCPA 1949) (Diligence requires that applicants must be specific as to dates and facts.).

Here, Appellants’ arguments and Declaration consist of general statements of due diligence. *See* Br. 8–9. Absent evidence or a showing of facts, this amounts to mere pleading. *See Borkowski*, 505 F.2d at 718; Ans. 22–23. Additionally, we agree with the Examiner that the submitted evidence and argument is insufficient to establish an actual (or constructive) reduction to practice prior to the Ilitzky reference. Ans. 19–20. In particular, the Examiner explains the Ph.D. research does not evidence a reduction to practice the invention, but rather proposes areas to be explored. Ans. 20 (citing Proposal Section 1.3).

For the reasons discussed *supra*, we are not persuaded the Examiner erred in finding Ilitzky is prior art to Appellants’ claimed invention. Appellants do not substantively address the Examiner’s findings regarding the disclosure of Ilitzky. Accordingly, we sustain the Examiner’s rejection of independent claim 1 and independent claim 15, which recites similar limitations. Further, we sustain the Examiner’s rejection of claims 2–8 and 16–21, which depend therefrom and were not argued separately. *See* Br. 8–9.

*Rejection of claims 9 and 22 under 35 U.S.C. § 103(a)*

Claims 9 and 22 depend from independent claims 1 and 15, respectively, and recite “wherein the bus is arranged to wake up units of the network on chip that have been shut off.” In rejecting claims 9 and 22, the Examiner finds, in addition to disclosing the limitations recited in the independent claims, “Ilitzky further discloses that the bus provides control data to the units of the network on chip.” Final Act. 9 (citing Ilitzky at 64–65). Additionally, the Examiner takes Official Notice that “powering off and waking up electronic units is notoriously old and well known in the art.” Final Act. 9. The Examiner explains in order to reduce the amount of power consumed by the chip by powering the unit only when units are needed, an ordinarily-skilled artisan would, therefore, power on and wake up the units of the network on chip using the bus. Final Act. 9.

Appellants admit that although powering up units is known in the art, a person having ordinary skill in the art would not wake the units of the network on chip by using the bus. Br. 9. Additionally, Appellants assert that the Examiner’s taking of Official Notice is contested, and not admitted. Br. 9.

To adequately traverse the Examiner’s taking of Official Notice, Appellants “must specifically point out the supposed errors in the [E]xaminer’s action.” MPEP § 2144.03C. If the assertion of Official Notice is not traversed, it “is taken to be admitted prior art.” *Id.*

Here, Appellants fail to specifically point out errors in the Examiner’s assertion of Official Notice. Additionally, Appellants admit “[p]owering up units is known in the art.” Br. 9. Further, the Examiner finds, and we agree, commands for powering off and waking up of units are control data, and

Ilitzky discloses that control data is transmitted over the bus. Ans. 25 (citing Ilitzky at 64–65). Thus, Ilitzky discloses sending command over the bus to power off and wake up units of the network on chip.

For the reasons discussed *supra*, we are unpersuaded of Examiner error. Accordingly, we sustain the Examiner’s rejection of claims 9 and 22.

*Rejection of claims 28 and 29 under 35 U.S.C. § 102(a)*

In addition to incorporating their arguments regarding the applicability of Ilitzky as a prior art reference, Appellants assert Ilitzky teaches a separation between the control plane and the network on chip data plane. Br. 10 (citing Ilitzky at 64–65). Appellants explain Ilitzky discloses the use of a separate control plane is used “to escape deadlocks caused by congestion in the NOC [(network on chip)].” Br. 10 (quoting Ilitzky at 65). Appellants assert, therefore, Ilitzky teaches away from the limitations of claims 28 and 29 and instead teaches “the control plane [(in Ilitzky)] is not used for data transfer.” Br. 11.

As an initial matter, we note Appellants’ argument of Ilitzky teaching away from Appellants’ claimed invention is irrelevant for a rejection under section 102. *Seachange Int’l, Inc., v. C-COR, Inc.*, 413 F.3d 1361, 1380 (Fed. Cir. 2005).

Further, we disagree with Appellants that the control plane of Ilitzky is not used for data transfer. As the Examiner explains, Ilitzky discloses using the bus (i.e., control plane) for time critical data—to avoid congestion on the network on card. Ans. 26 (citing Ilitzky at 65). Additionally, the Examiner notes, as do we, the claims refer to “data transactions.” Ans. 26. Because control signals are a type of data, we agree with the Examiner that

Ilitzky discloses using the bus to send time-critical data. Ans. 26. The Examiner also explains “[b]ecause congestion is possible in the NoC (See Page 65), data sent across it would necessarily be non-time-critical, as the time critical data is sent across the point-to-point bus control plane.”

Ans. 26. Appellants do not persuasively rebut the Examiner’s findings or reasoning.

For the reasons discussed *supra*, we are unpersuaded of Examiner error. Accordingly, we sustain the Examiner’s rejection of claims 28 and 29.

*Rejection of claims 10–14 and 23–27 under 35 U.S.C. § 103(a)*

Appellants do not present separate arguments of patentability rebutting the Examiner’s rejection of claims 10–14 and 23–27. Accordingly, we summarily sustain the Examiner’s rejection of these claims.

*Rejection of claims 1–4, 7, 15–18, and 20 under 35 U.S.C. § 103(a)*

Alternatively, the Examiner also rejected independent claims 1 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Kang and Tufford. Final Act. 12–15. Appellants assert Kang is directed to providing a network on chip solution to the problems imposed by buses and, therefore, teaches away from using a bus in parallel to the network on chip, as claimed. Br. 12–14 (citing Kang ¶¶ 1–5, 7). Additionally, Appellants argue Tufford teaches the use of a switched fabric and not network on chip. Br. 14. Appellants argue one of ordinary skill in the art would not have been motivated to combined Kang and Tufford. Br. 14.

Contrary to Appellants’ assertions, the Examiner finds Kang does not teach away from using a bus in parallel with a network on chip. Ans. 27.

The Examiner explains that Kang merely discloses one would not want to use a bus *instead of* a network on chip. Ans. 27. In other words, Kang does not discredit or discourage a combination of a bus and network on chip solution.

“A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.” *In re Kubin*, 561 F.3d 1351, 1357 (Fed. Cir. 2009) (citation omitted). The identified sections of Kang appear in the Background of Kang’s Specification and serve to juxtapose certain issues associated with a bus (e.g., scalability, bandwidth, and synchronization) as compared to a network on chip approach. *See* Kang ¶ 3. Further, Kang states that with use of network on chip “it is expected to be possible to solve [these issues] . . . [but] many investigations” are still required to determine its efficacy. Kang ¶ 4. Thus, we agree with the Examiner that Kang does not teach away from being combined with Tufford.

Additionally, we find Appellants’ argument that Tufford teaches a switched fabric rather than a network on chip to be unpersuasive as it is not responsive to the Examiner’s rejection. The Examiner relies on Kang, not Tufford, to teach a network on chip solution. *See* Final Act. 13 (citing Kang ¶ 38, Fig. 1).

The Examiner also explains Tufford teaches “implementing a bus in parallel to a network to a plurality of network modules, wherein a latency of the bus is lower and more predictable than a latency of the network. Ans. 27 (citing Tufford ¶¶ 13–19, Fig. 1). Further, the Examiner finds the

combination of Tufford's parallel bus and network with Kang's network would yield the predictable result of increasing the speed of the system. Ans. 27 (citing Tufford ¶ 18). Appellants do not provide sufficient, persuasive evidence or argument to rebut the Examiner's finding and reasoning.

For the reasons discussed *supra*, we are unpersuaded of Examiner error. Accordingly, we sustain the Examiner's rejection under 35 U.S.C. § 103(a) of independent claim 1 and, for similar reasons, the rejection of independent claim 15, which recites similar limitations. Additionally, we sustain the Examiner's rejection of claims 2–4, 7, 16–18, and 20, which were not argued separately. *See* Br. 14.

*Rejection of claims 5, 6, 9, 19, and 22 under 35 U.S.C. § 103(a)*

Appellants advance similar arguments to those already presented. *See* Br. 14–15. In particular, Appellants contend a person having ordinary skill in the art would not have been motivated to combine the teachings of Kang and Tufford. Br. 14. Additionally, Appellants assert that although powering up units is known in the art, a person having ordinary skill in the art would not wake the units of the network on chip by using the bus and that the Examiner's taking of Official Notice is contested, and not admitted. Br. 15.

For the reasons discussed previously, we find these arguments unpersuasive of Examiner error. Accordingly, we sustain the Examiner's rejection of claims 5, 6, 9, 19, and 22.

*Rejection of claims 28 and 29 under 35 U.S.C. § 103(a)*

Appellants argue Tufford does not teach “a bus that conveys time-critical point to point data transactions and the network on chip conveys non time-critical point to point data transactions.” Br. 15. Instead, Appellants assert Tufford teaches a multi-drop bus acting as a separate control plane and a switched fabric operating as a data plane. Br. 16 (citing Tufford ¶¶ 14–18). Appellants conclude Tufford “teach[es] away from claims 28 and 29.” Br. 16.

As discussed previously, Appellants’ arguments of a separate control plane do not persuade us of Examiner error. As the Examiner explains, Tufford teaches the control plane is used for “synchronization, organization, and management control data.” Ans. 29–30 (citing Tufford ¶ 18). The Examiner finds this control data is “necessarily time-critical.” Ans. 29. The Examiner further finds all other data, including non-time-critical data, is sent over the network. Ans. 30. Appellants do not persuasively rebut the Examiner’s findings. Accordingly, we sustain the Examiner’s rejection of claims 28 and 29.

*Rejection of claims 8, 10–14, 21, and 23–27 under 35 U.S.C. § 103(a)*

Appellants do not present separate arguments of patentability rebutting the Examiner’s rejection of claims 8, 10–14, 21, and 23–27 as being unpatentable over Kang, Tufford, and Coll. Accordingly, we summarily sustain the Examiner’s rejection of these claims.

DECISION

We affirm the Examiner's decision to reject claims 1–8, 15–21, 28, and 29 under 35 U.S.C. § 102(a).

We affirm the Examiner's decision to reject claims 9–14 and 22–27 under 35 U.S.C. § 103(a) as being unpatentable over Ilitzky and Coll.

We affirm the Examiner's decision to reject claims 1–29 under 35 U.S.C. § 103(a) as being unpatentable over Kang, Tufford, and Coll.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

AFFIRMED