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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ERAN PISEK, SHADI ABU-SURRA, and
THOMAS M. HENIGE

Appeal 2015-002855
Application 13/248,900
Technology Center 2100

Before BRADLEY W. BAUMEISTER, JOSEPH P. LENTIVECH, and
AMBER L. HAGY, *Administrative Patent Judges*.

BAUMEISTER, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's
Final Rejection of claims 1–9. App. Br. 6.¹ Claims 10–24 stand withdrawn
from consideration. *Id.* We reverse.

¹ Rather than repeat the Examiner's positions and Appellants' arguments in their entirety, we refer to the following documents for their respective details: the Final Action mailed February 5, 2014; the Appeal Brief filed September 2, 2014; the Examiner's Answer mailed October 9, 2014 ("Ans."); and the Reply Brief filed December 9, 2014 ("Reply Br.").

STATEMENT OF CASE

Appellants describe the present invention as follows:

An apparatus and method decode LDPC code. The apparatus includes a memory and a number of LDPC processing elements. The memory is configured to receive a LDPC codeword having a length equal to a lifting factor times a base LDPC code length, wherein the lifting factor is greater than one. The number of LDPC processing elements configured to decode the LDPC codeword, wherein each of the number of LDPC processing elements decode separate portions of the LDPC codeword.

Abstract.

Independent claim 1, reproduced below, is illustrative of the appealed claims:

1. An apparatus for decoding a low density parity check (LDPC) code, the apparatus comprising:

a memory configured to receive a LDPC codeword having a length equal to a lifting factor times a base LDPC code length, wherein the lifting factor is greater than one; and

a number of LDPC processing elements configured to decode the LDPC codeword, wherein each of the number of LDPC processing elements decode separate portions of the LDPC codeword,

wherein, when the LDPC processing elements decode in parallel, a first LDPC processing element in the LDPC processing elements is configured to receive the LDPC codeword and decode a fraction of a total number of rows in the LDPC code, the fraction equal to one over the number of the LDPC processing elements.

Claims 1–9 stand rejected under 35 U.S.C. § 103(a) as obvious over Richardson (US 2009/0063933 A1; published Mar. 5, 2009) in view of Rhee (US 6,854,082 B1; issued Feb. 8, 2005).

We have jurisdiction under 35 U.S.C. § 6(b). We review the appealed rejections for error based upon the issues identified by Appellants, and in light of the arguments and evidence produced thereon. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential).

CONTENTIONS

The Examiner finds that Richardson teaches an apparatus for decoding a low density parity check (LDPC) code that comprises a memory and a plurality of processing elements configured to decode the LDPC codeword. Final Act. 4. The Examiner finds that Richardson does not teach the last limitation of independent claim 1:

Richardson does not explicitly teach each of the number of LDPC processing elements decode separate portions of the LDPC codeword wherein, when the LDPC processing elements decode in parallel, a first LDPC processing element in the LDPC processing elements is configured to receive the LDPC codeword and decode a traction of a total number of rows in the LDPC code, the fraction equal to one over the number of the LDPC processing elements.

Id. at 4–5.

The Examiner additionally finds that this missing disclosure is taught by Rhee and that motivation existed to combine these teachings of Rhee with those of Richardson. *Id.* at 5–6. More specifically, the Examiner finds that Rhee’s FIG 2 embodiment includes four LDCU processing units 30, 32, 34, and 36, each of which corresponds to the claimed LDPC processing elements. Ans. 9–10. The Examiner further finds that each of Rhee’s LDCU processing units has a right and left decoding subsection (e.g., Rhee’s LDPC processing element 30 has left half and right half decoding subsections LH DU A 38 and RH DU A 40). *Id.* at 10.

The Examiner finds that each of these subsections receives a codeword and decodes a one-half fraction thereof. *Id.* at 10–11. As such, then, the Examiner finds that each of Rhee’s subsections (e.g., LDHU A 38) corresponds to the claimed “first LDPC processing element.” *Id.* at 10.

Appellants contend, *inter alia*, that Rhee fails to disclose an LDPC processing element that receives the entire codeword, but then decodes only a fraction of the total number of rows in the LDPC code. App. Br. 16.

ANALYSIS

Appellants’ arguments are convincing. As noted above, the Examiner first interprets Rhee’s entire decoder section (e.g., decoder section 30) as corresponding to one of the claimed LDPC processing elements that receives an entire codeword. Then the Examiner shifts position, alternatively interpreting each of the decoder sections’ subsections (e.g., LHDU A 38) as corresponding to each of the claimed LDPC processing elements. The Examiner does not, however, point to any single component of Rhee that first receives an entire codeword and then decodes only a portion of it. In fact, Rhee alternatively teaches that while each of the decoder sections 30, 32, 34, and 36 receive the entire signal vector, y , the signal is broken into left and right halves y_L , y_R , which sub-codes are then routed *respectively* to the left hand and right hand decoder units (e.g., LHDU A 38, RHDU A 40). Rhee col. 5, l. 35–col. 6, l. 6, *cited in* PO App. Br. 15–16.

For the foregoing reasons, Appellants have persuaded us of error in the Examiner’s obviousness rejection of independent claim 1. Accordingly, we will not sustain the Examiner’s rejection of that claim or of claims 2–9, which depend from claim 1.

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DECISION

The Examiner's decision rejecting claims 1–9 is reversed.

REVERSED