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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* JAMES HUFFMAN, DARREN KAUFMAN,  
and DOUGLAS MEDINA<sup>1</sup>

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Appeal 2015-001754  
Application 11/943,877  
Technology Center 2400

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Before JEFFREY S. SMITH, JOHN F. HORVATH, and  
MICHAEL M. BARRY, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1–13, 15, 16, 18, 20, and 22, which constitute all pending claims. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART and, pursuant to our authority under 37 C.F.R. § 41.50(b), enter NEW GROUNDS OF REJECTION.

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<sup>1</sup> Appellants identify the real party in interest as AT&T Intellectual Property I, L.P. (App. Br. 2.)

*Introduction*

Appellants state their “disclosed subject matter relates generally to instrumentation for monitoring the transmission quality of digital signals and, more particularly, digital multimedia content signals.” (Spec ¶ 1.)

CLAIMED SUBJECT MATTER

Claim 1 is illustrative:

1. A multimedia signal monitoring unit, comprising a chassis and within the chassis:

a processor;

a multimedia signal receiver for receiving a modulated multimedia stream;

a plurality of demodulating chip sets and a corresponding plurality of selectable demodulating algorithms, wherein each of the demodulating algorithms is implemented in its corresponding chip set and is suitable for demodulating the modulated multimedia stream;

an analysis module to determine transmission quality signal characteristics of demodulated multimedia streams from the demodulating algorithms; and

a switch under control of the processor, wherein the switch is configured to connect the multimedia signal receiver to a selected one of the demodulating algorithms.

(App. Br. 14 (Claims App’x).)

*References and Rejections*

Claims 1–9, 11–13, 15, 16, 18, and 22 stand rejected under 35 U.S.C. § 103(a) as obvious over Sampath (US 8,223,904 B2; July 17, 2012) and Vysotsky et al. (US 2006/0168637 A1; July 27, 2006) (“Vysotsky”). (Final Act. 3–10.)

Claims 10 and 20 stand rejected as obvious over Sampath, Vysotsky, and Locket et al. (US 2008/0288998 A1; Nov. 20, 2008). (Final Act. 11–12.)

ISSUES<sup>2</sup>

(1) Does the Examiner err in rejecting claim 1 because Sampath and Vysotsky “fail to teach or suggest a plurality of demodulating chip sets and a corresponding plurality of selectable demodulating algorithms, wherein each of the demodulating algorithms is implemented in its corresponding chip set as recited . . . .”? (App. Br. 4–5.)

(2) Does the Examiner err in rejecting claim 3 by finding Sampath teaches or suggests “a plurality of circuit boards,” as recited? (*Id.* at 8.)

(3) Does the Examiner err in rejecting claim 4 by finding Vysotsky teaches or suggests “each of the circuit boards is received within a corresponding slot defined within the chassis,” as recited? (*Id.* at 8–9.)

(4) Does the Examiner err in rejecting claim 5 by finding Vysotsky’s “single board system” teaches or suggests “a plurality of boards being swapable among a plurality of slots,” as recited? (*Id.* at 9.)

(5) Does the Examiner err in rejecting claim 12 by finding “the simultaneously transcoding of a signal according to two or more video signal formats” in Vysotsky teaches or suggests “the claimed feature of implementing two different revisions of a demodulating algorithm in two different chip sets?” (*Id.* at 9–10.)

(6) Does the Examiner err in rejecting independent claim 16 because Vysotsky and Sampath fail to teach or suggest the recited requirements? (*Id.* at 11.)

(7) Does the Examiner err in rejecting claim 22 by finding Vysotsky teaches “the transmission quality signal characteristic (of claim 16) is

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<sup>2</sup> Appellants present no separate arguments for the patentability of claims 2, 6–11, 13, 15, 18, and 20. (*See* App. Br. 4–12.)

selected from a signal to noise ratio of the signal and a packet error rate associated with the signal,” as recited? (*Id.* at 12.)

## ANALYSIS

### *Claim 1*

Appellants argue the Examiner errs in rejecting claim 1 because Vysotsky and Sampath do not teach or suggest the recited “plurality of demodulating chip sets and a corresponding plurality of selectable demodulating algorithms.” (App. Br. 4–8; *see also* Reply Br. 2–3.) Appellants contend “Sampath makes no reference to or mention of a chip set, let alone an embodiment in which each of a plurality of chip sets implements a corresponding demodulating algorithm.” (App. Br. 5.) Appellants further argue this feature is not inherent in Sampath (App. Br. 5–7) and that the Examiner errs by failing “to indicate *how* Sampath teaches or suggests the chip set per algorithm feature of claim 1” (Reply Br. 3 (emphasis added).)

Appellants do not persuade us of Examiner error. The Examiner finds, and we agree, that Sampath’s disclosure that its demodulating algorithms may be implemented in various types of hardware, such as different combinations of processors, programmable logic devices or gate arrays, etc., teaches or suggests the use of chip sets as claimed to one of ordinary skill. (*See* Final Act. 4, Ans. 11–12 (citing Sampath Figs. 2–3, col. 8:12–65).) Furthermore, we note that Vysotsky teaches embodiments with multiple encoder/decoder pairs, each of which “may be dedicated to one or a limited number of compression schemes” (Vysotsky ¶ 106; *see* Figs. 1a–4) and it is “possible to create a video and audio encoder/decoder pair within the scope of a physically small single board-level system” (Vysotsky ¶ 48).

We find one of ordinary skill understands the embodiments in figures 1–6d of Vysotsky can include “single board systems” for each of the encoder/decoder pairs. We note that Vysotsky’s discussion of a “stand-alone” single board system does not negate its teachings regarding the use of multiple single board encoder/decoder pairs within a system.

We find that either Sampath alone, or Sampath in combination with Vysotsky, teaches or suggests claim 1’s “plurality of demodulating chip sets” requirements. *See, e.g., KSR Int’l co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (noting an obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, as the analysis can take account of the inferences and creative steps that a person of ordinary skill in the art would employ).

We accordingly sustain the rejection of claim 1. We also sustain the rejection of its dependent claims 2, 6, and 7, for which Appellants provide no separate arguments.

To give Appellants a full and fair opportunity to respond to the thrust of the rejection of claim 1 as supplemented by our findings and reasoning above, we designate the rejections of claims 1, 2, 6, and 7 as a new ground of rejection. We incorporate into this new ground of rejection the Examiner’s findings and reasons in the rejection of claims 1, 2, 6, and 7, except for the “analysis module” and “switch” limitations. (*See* Final Act. 3–6.) Claim 16 includes “analysis module” and “switch” limitations similar to those of claim 1, which we address below.<sup>3</sup> We incorporate our findings

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<sup>3</sup> Unlike for claim 16, Appellants do not argue the Examiner errs in the rejection of claim 1 based on the “analysis module” requirements. Arguments not made are waived. *See* 37 C.F.R. § 37.41(c)(iv).

and conclusions below for the “analysis module” and “switch” limitations of claim 16 into the new ground of rejection for claims 1, 2, 6, and 7. That is, claim 11 of Sampath teaches the “analysis module” and “switch” limitations of these claims, including a “means for deciding based on a metric” and “wherein the metric is a signal to interference-plus-noise” ratio (SINR).” (Sampath, 10:17–22.)

### *Claims 3–5*

Appellants argue the Examiner errs in finding Sampath teaches claim 3’s requirement that each of the chip sets recited in claim 1 is attached to a corresponding circuit board. We agree Sampath does not teach this and, accordingly, do not sustain the Examiner’s rejection. Vysotsky, however, teaches or suggests the added requirement of claim 3 by its disclosure of the use of multiple “single board” systems that have an encoder/decoder pair that each support a single compression standard (*see* Vysotsky ¶¶ 47–48; Figs. 1a–6d) along with the use of such multiple encoder/decoder pairs in a single system (*see, e.g.*, Vysotsky ¶¶ 52–53). We accordingly conclude claim 3 is obvious over Sampath and Vysotsky; we designate this as a new ground of rejection, incorporating our findings for claim 1, discussed *supra*, into our rejection of claim 3, which depends from claim 1.

Claim 4 adds “wherein each of the circuit boards is received within a corresponding slot defined within the chassis” to claim 3. Because we do not sustain the Examiner’s rejection of claim 3, we also do not sustain the Examiner’s rejection of claim 4. We note, however, that Vysotsky teaches multiple system configurations and “the system can be implemented with standard signal connectors rather than bus-based I/O connections so as to provide stand-alone implementation without physical installation in a host

system chassis.” (Vysotsky ¶ 28.) Vysotsky thus teaches that physical installation of the encoder/decoder pairs as “single board” systems in a host system chassis is clearly an option. The use of slots in a chassis for installation of boards is notoriously well known. See, for example, the discussion of the NuBus architecture *infra*. We find Vysotsky’s disclosure of installing multiple boards teaches or suggests the added requirements of claim 4. We accordingly conclude claim 4 is obvious over Sampath and Vysotsky; we designate this as a new ground of rejection, incorporating our findings for claim 3, discussed *supra*, into our rejection of claim 4, which depends from claim 3.

Claim 5 adds “wherein the circuit boards are swappable among the slots” to claim 4. Because we do not sustain the Examiner’s rejection of its parent claim, we also do not sustain the rejection of claim 5. Use of a chassis with a backplane having slots that interchangeably accept circuit boards is, however, notoriously well known in the art. For example, the NuBus architecture, later standardized as IEEE 1196 in 1987, enables “plug-and-play” functionality for “slot agnostic” circuit boards. (See <http://web.archive.org/web/20041014214859/http://en.wikipedia.org/wiki/NuBus>.) We find the NuBus prior art teaches the added requirement of claim 5 and, because of the efficiency and versatility such functionality provides, that one of ordinary skill would have been motivated to combine its teachings with the teachings of Sampath and Vysotsky. We accordingly conclude claim 5 is obvious over the combination of the NuBus architecture with Sampath and Vysotsky; we designate this as a new ground of rejection, incorporating our findings for claim 4, discussed *supra*, into our rejection for claim 5, which depends from claim 4.

*Claims 8–11 and 15*

Independent claim 8 recites requirements analogous to the combined requirements of claims 1, 3, and 4. For the same reasons we do not sustain the rejections of claims 3 and 4, we do not sustain the rejection of claim 8, along with its dependent claims 9–13 and 15. We designate a new ground of rejection for claim 8 as obvious over Sampath and Vysotsky on the same, combined basis for the new grounds of rejection discussed above for claims 1, 3, and 4. In particular, we find Vysotsky teaches systems having a first chipset housed on a first printed circuit board executing a first algorithm (e.g., Sampath’s demodulating algorithm), and a second chipset housed on a second printed circuit board executing a second algorithm were well known in the art. (*See* Vysotsky ¶¶ 28, 47–48, 52–53, 106, Figs. 1a–4.) We also find Sampath teaches it was well known to include in such systems an analysis module to analyze transmission quality signal characteristics, and a switch to select one of the demodulation algorithms executing on one of the circuit boards. (*See* Sampath 10:17–22, Fig. 5A (deciding means and first and second demodulation means).)

We similarly designate a new ground of rejection for claims 9, 11–13, and 15 as obvious over Sampath and Vysotsky on the same basis as for the new grounds of rejection discussed above for claim 8, from which these claims depend, and the Examiner’s particular findings regarding claims 9, 11–13, and 15 from the Final Action. (*See* Final Act. 7–9.) In addition, regarding the rejection of 15, we find that Sampath teaches the analysis module determines an error rate associated with the media stream. (*See* Sampath 10:3–12, 10:26–28 (where the validity check is a decryption error check).)

We also designate a new ground of rejection for claim 10 as obvious over Sampath, Vysotsky, and Locker on the same basis for the new grounds of rejection discussed above for claim 8, from which these claims depend, and the Examiner's particular findings regarding the teachings of Locket from the Final Action. (*See* Final Act. 11.)

*Claims 12 and 13*

Claim 12 requires each of two circuit boards to generate ATSC (Advanced Television Systems Committee) compliant signals based on different revisions of the same demodulating algorithm. (*See* App. Br. 16 (Claims App'x).) Appellants argue the Examiner errs in rejecting claim 12 because "the Examiner's attempt to equate or analogize [Vysotsky's] simultaneously transcoding of a signal according to two or more video signal formats with the claimed feature of implementing two different revisions of a demodulating algorithm in two different chip sets is fatally flawed." (App. Br. 9–10 (citing Vysotsky ¶¶ 201, 216).) We agree and, accordingly, do not sustain the rejection of claim 12.

Appellants' Specification, however, states that using multiple ATSC decoding versions in different chip sets was known in the prior art. (Spec. ¶ 2 ("Description of the Related Art") ("Currently there are five different generations of ATSC decoder chip sets. A consumer or commercial receiver may use any one of the five generations of chip sets.").) We find that, in view of the teachings of Sampath and Vysotsky, this admitted prior art teaches one of ordinary skill the added requirements of claim 12. We accordingly conclude claim 12 is obvious over its combination with Sampath and Vysotsky; we designate this as a new ground of rejection,

incorporating our findings regarding claims 8 and 11, discussed *supra*, from which claim 12 depends.

Because we do not sustain the rejection of claim 12, we also do not sustain the rejection of its dependent claim 13. We designate new grounds of rejection for claim 13 as obvious over the combination of Sampath and Vyotsky for the same reasons discussed above regarding claim 12.

*Claim 16, 18, and 20*

Claim 16 is an independent claim and recites “a monitoring unit” with requirements directed to a chassis with slots, circuit boards with chips for executing demodulating algorithms, a receiver, an analysis module, and a switch for connecting a received signal to a selected circuit board. (*See App. Br. 16–17 (Claims App’x).*) Appellants argue the Examiner errs in relying on Vysotsky’s “alleged description of controlling a switch matrix based on an analysis of the type of content received for teaching [the] claimed feature of analyzing transmission quality characteristics.” (*App. Br. 11.*)

We agree with Appellants that Vysotsky does not teach claim 16’s recited “analysis module” requirement “to analyze transmission quality signal characteristics of demodulated multimedia streams produced by the circuit boards” and, accordingly, do not sustain the Examiner’s rejection of claim 16, along with its dependent claims 18 and 20.

Sampath’s claim 11, however, which includes the requirements of its parent claims 8 and 10<sup>4</sup>, discloses a “multiple-input receiver . . . wherein the

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<sup>4</sup> Claim 11 depends from independent claim 8, which recites a “means for deciding between the first and second algorithm to produce a modulated

metric is a signal to interference-plus-noise ratio (SINR)” (Sampath 10:20–22). Thus, Sampath teaches analyzing SINR (a transmission quality signal characteristic of the demodulated signals) as a means for deciding which demodulation algorithm to use. Sampath further teaches a means for deciding between the first and second demodulation algorithms (e.g., running on different circuit boards as taught by Vysotsky), and therefore teaches a switch operable to identify a selected circuit board as recited in claim 16. (*Id.* at 10:17–19, Fig. 5A (deciding means).) We find these disclosures teach claim 16’s “analysis module” and “switch” limitations, and conclude that claim 16 is obvious over the combined teachings of Sampath<sup>5</sup> and Vysotsky. We designate this as a new ground of rejection.

We similarly designate a new ground of rejection for claim 18 as obvious over Sampath and Vysotsky on the same basis for the new grounds of rejection discussed above for claim 16, from which claim 18 depends, and the Examiner’s particular findings regarding claim 18 found in the Final Action. (*See* Final Act. 10.) We also designate a new ground of rejection for claim 20 as obvious over Sampath, Vysotsky, and Lockett on the same basis as for the new ground of rejection discussed above for claim 16, from

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signal,” and dependent claim 10, which recites “the means for deciding [is] based at least in part on a metric”. (Sampath 8:59–9:10.)

<sup>5</sup> Appellants further argue the Examiner errs in relying on Sampath “for teaching multiple circuit boards, each including a respective version of a chip set” (App. Br. 11). This limitation is analogous to the limitation of claim 3 (which depends from claim 1). We incorporate the findings and reasons discussed *supra* for the new grounds of rejection of claims 1 and 3 into our determination that claim 16 is obvious, namely, Vysotsky teaches systems with a plurality of circuit boards, each executing respective demodulation/decoding algorithms on dedicated chip sets, were known in the art. (*See* Vysotsky ¶¶ 28, 47–48, 52–53, 106, Figs. 1a–4.)

which claim 20 depends, and the Examiner's particular findings regarding the teachings of Locker found in the Final Action. (*See* Final Act. 11–12.)

### *Claim 22*

Claim 22 depends from claim 16 and recites “wherein the transmission quality signal characteristic is selected from a signal to noise ratio of the signal and a packet error rate associated with the signal.” (App. Br. 17 (Claims App’x).) Appellants argue the Examiner errs in relying on Vysotsky for teaching the requirements of claim 22. (App. Br. 12.) We agree and, accordingly, do not sustain the rejection. As discussed *supra* for claim 16, however, we find that Sampath’s claim 11 specifically discloses analyzing a signal-to-noise ratio as a transmission quality characteristic. Accordingly, we conclude claim 22 is obvious over the combination of Sampath and Vysotsky. We designate this as a new ground of rejection, incorporating our findings regarding claim 16, discussed *supra*, from which claim 22 depends.

### DECISION

For the above reasons, we affirm the rejection of claims 1, 2, 6, and 7, and we reverse the rejection of claims 3–5, 8–13, 15, 16, 18, 20, and 22. Pursuant to our authority under 37 C.F.R. § 41.50(b), we enter new grounds of rejection for claims 1, 3–5, 8–13, 15, 16, 18, 20, and 22 as obvious under 35 U.S.C. § 103(a).

Section 41.50(b) provides “[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review.” Section 41.50(b) also provides:

When the Board enters such a non-final decision, the appellant, within two months from the date of the decision,

must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

(1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new Evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the prosecution will be remanded to the examiner. The new ground of rejection is binding upon the examiner unless an amendment or new Evidence not previously of Record is made which, in the opinion of the examiner, overcomes the new ground of rejection designated in the decision. Should the examiner reject the claims, appellant may again appeal to the Board pursuant to this subpart.

(2) Request rehearing. Request that the proceeding be reheard under § 41.52 by the Board upon the same Record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

Further guidance on responding to a new ground of rejection can be found in the Manual of Patent Examining Procedure § 1214.01.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART  
37 C.F.R. § 41.50(b)